

# **EXHIBIT 1**

US006429481B1

(12) **United States Patent**  
**Mo et al.**(10) **Patent No.: US 6,429,481 B1**  
(45) **Date of Patent: \*Aug. 6, 2002**(54) **FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE**(75) Inventors: **Brian Sze-Ki Mo**, Fremont; **Duc Chau**, San Jose; **Steven Sapp**, Felton; **Izak Bencuya**, Saratoga, all of CA (US); **Dean Edward Probst**, West Jordan, UT (US)(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, MA (US)

(\*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

4,345,265 A	8/1982	Blanchard .....	357/23
4,398,339 A	8/1983	Blanchard et al. ....	29/571
4,503,449 A	3/1985	David et al. ....	357/23.4
4,503,598 A	3/1985	Vora et al. ....	29/571
4,541,001 A	9/1985	Schutten et al. ....	357/23.4
4,639,762 A	1/1987	Neilson et al. ....	357/23.8

(List continued on next page.)

**FOREIGN PATENT DOCUMENTS**

EP	0238749	9/1987
EP	0550770	7/1993
EP	0583028 A1	2/1994

(List continued on next page.)

**OTHER PUBLICATIONS**S. M. Sze: "P-N-Junction Diode" *Physics of Semiconductor Devices Second Edition Bell Laboratories*, pp. 63-108 (1981).

(List continued on next page.)

(21) Appl. No.: **08/970,221**(22) Filed: **Nov. 14, 1997**(51) **Int. Cl.<sup>7</sup>** ..... **H01L 29/78**(52) **U.S. Cl.** ..... **257/341; 257/331**(58) **Field of Search** ..... **257/330, 245, 257/497, 618, 341, 331**(56) **References Cited****U.S. PATENT DOCUMENTS**

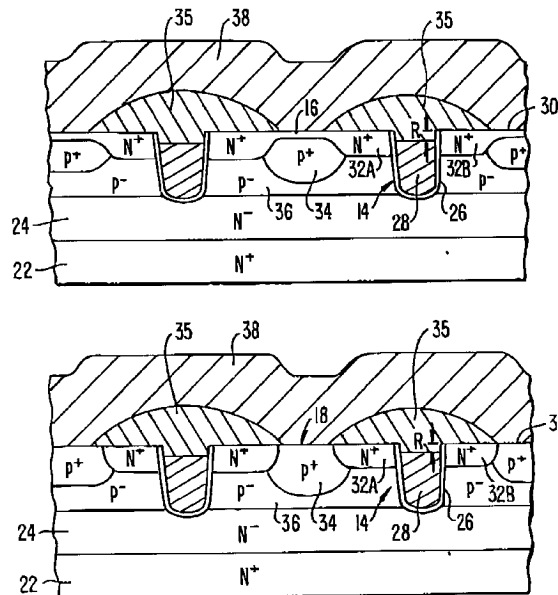
4,070,690 A	1/1978	Wickstrom .....	357/68
4,132,998 A	1/1979	Dingwall .....	357/23
4,145,703 A	3/1979	Blanchard et al. ....	357/55
4,326,332 A	4/1982	Kenney .....	
4,329,705 A	5/1982	Baker .....	357/43
4,344,081 A	8/1982	Pao et al. ....	357/43

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(57) **ABSTRACT**

A trench field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

**22 Claims, 9 Drawing Sheets**

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U.S. PATENT DOCUMENTS								
4,682,405	A	7/1987	Blanchard et al. ....	29/571	EP	0720236	3/1996	
4,683,643	A	8/1987	Nakajima et al. ....	437/203	EP	0746030	4/1996	
4,767,722	A	8/1988	Blanchard .....	437/41	EP	0 720 236	7/1996	..... H01L/29/78
4,808,543	A	2/1989	Parrillo et al. ....	437/38	EP	0 746 030	12/1996	..... H01L/27/02
4,845,537	A	7/1989	Nishimura et al.		EP	0 755 076	1/1997	..... H01L/29/739
4,860,072	A	8/1989	Zommer .....	357/23.8	EP	0755076	1/1997	
4,881,105	A	11/1989	Davari et al.		EP	0 795 911	9/1997	..... H01L/29/739
4,893,160	A	1/1990	Blanchard .....	357/23.4	EP	0795911	9/1997	
4,914,058	A	4/1990	Blanchard .....	437/203	EP	0801425	10/1997	
4,967,245	A	10/1990	Cogan et al. ....	357/23.4	EP	0 801 425	10/1997	..... H01L/29/10
4,983,535	A	1/1991	Blanchard .....	437/40	GB	2 269 050	1/1994	..... H01L/29/06
5,016,068	A	5/1991	Mori .....	357/23.5	GB	2269050 A	1/1994	
5,017,504	A	5/1991	Nishimura et al.		GB	2 269 050 A	1/1994	
5,045,900	A	9/1991	Tamagawa .....	357/23.4	JP	56131960	10/1981	
5,072,266	A	12/1991	Bulucea et al.		JP	57018365	1/1982	
5,124,764	A	6/1992	Mori .....	357/23.4	JP	57153469	9/1982	
5,160,491	A	11/1992	Mori .....	437/40	JP	58137254	8/1983	
5,168,331	A	12/1992	Yilmaz .....	257/331	JP	58210678	12/1983	
5,298,442	A	3/1994	Bulucea et al. ....	437/40	JP	59080970	5/1984	
5,298,780	A	3/1994	Harada		JP	59193064	11/1984	
5,316,959	A	5/1994	Kwan et al. ....	437/40	JP	60028271	2/1985	
5,341,011	A	8/1994	Hshieh et al. ....	257/330	JP	61102782	5/1986	
5,405,794	A	4/1995	Kim		JP	62012167	1/1987	
5,410,170	A	4/1995	Bulucea et al. ....	257/332	JP	62016572	1/1987	
5,430,324	A	7/1995	Bencuya		JP	62023171	1/1987	
5,455,190	A	10/1995	Hsu .....	437/40	JP	62046569	2/1987	
5,468,982	A	11/1995	Hshieh et al. ....	257/331	JP	63114173	5/1988	
5,474,943	A	12/1995	Hshieh et al. ....	437/40	JP	40 5-226661	* 9/1993	..... 257/330
5,508,534	A	4/1996	Nakamura et al.		JP	08204194	8/1996	
5,532,179	A	7/1996	Chang et al. ....	437/40	JP	08250731	9/1996	
5,541,425	A	7/1996	Nishihara		JP	08316479	11/1996	
5,558,313	A	9/1996	Hshieh et al. ....	257/342	JP	09036362	2/1997	
5,567,634	A	10/1996	Hébert et al.		JP	09102607	4/1997	
5,578,851	A	11/1996	Hshieh et al. ....	257/330	JP	09270512	10/1997	
5,592,005	A	1/1997	Floyd et al. ....	257/331	WO	9303502	2/1993	
5,597,765	A	1/1997	Yilmaz et al. ....	437/203	WO	9534094	12/1995	
5,602,046	A	2/1997	Calafut et al. ....	437/41	WO	9707547	2/1997	
5,605,852	A	2/1997	Bencuya .....	437/40	WO	WO 97/16853	5/1997	..... H01L/29/10
OTHER PUBLICATIONS								
Homes, F. E.; Salama, C. A. T., "V Groove M.O.S. Transistor Technology," Electronic letters vol. 9, No. 19 (Sep. 20, 1973).								
Homes, F. E.; Salama, C. A. T., "VMOS—A New MOS Integrated Circuit Technology," Solid-State Electronics, vol. 17, pp. 791–797 (1974).								
Ou–Yang, Paul, "Double Ion Implanted V–MOS Technology," IEEE Journal of Solid–State Circuits, vol. SC–12, No. 1, pp. 3–10 (Feb. 1977).								
Salama, C. Andre; Oakes, James G., "Nonplanar Power Field–Effect Transistor," IEEE Transactions on Electron Devices, vol. ED–25, No. 10, pp. 1222–1228 (Oct. 1978).								
Lisiak, Kenneth P.; Berger, Josef, "Optimization of Nonplanar Power MOS Transistors," IEEE Transactions on Electron Devices, vol. ED–25, No. 10, pp. 1229–1234 (Oct. 1978).								
Chang, T.S., et al, "Vertical FET Random–Access Memories with Deep Trench Isolation," IBM Technical Disclosure Bulletin, pp. 3683–3687 (Jan. 1980).								
Sun, S. C., "Physics and Technology of Power MOSFETs," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696–1 (Feb. 1982).								
FOREIGN PATENT DOCUMENTS								
EP	0 698 919	2/1996	.....	H01L/21/336				
EP	0698919	2/1996						
EP	0720235	3/1996						

**US 6,429,481 B1**

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Blanchard, Richard A., "Optimization of Discrete High Power MOS Transistors," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696-2 (Apr. 1982).

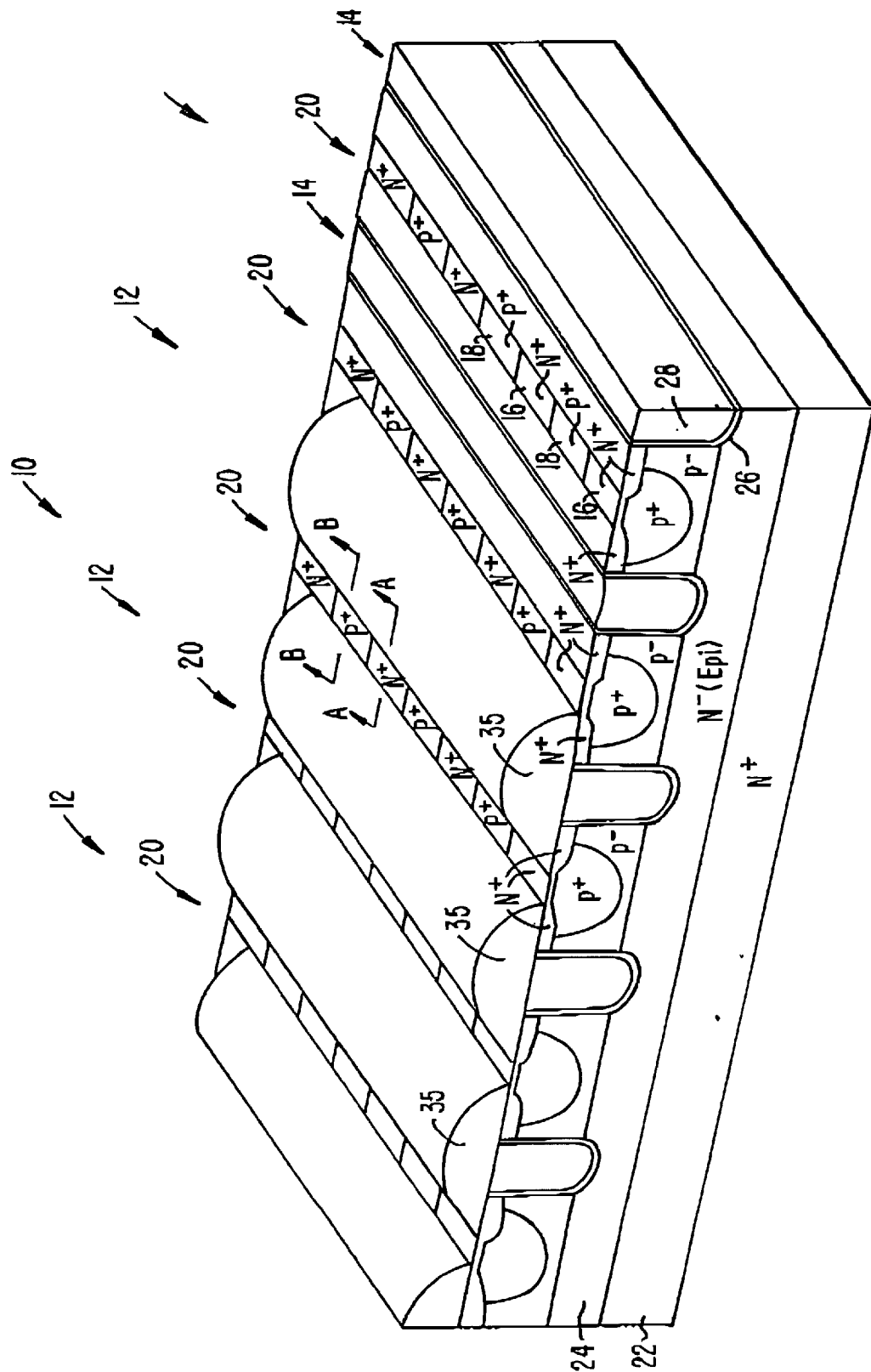
Frank Goodenough, Dense MOSFET Enables Portable Power Control, "Tech Insights", *Electronic Design*, Apr. 14, 1997.

Grant, D.A., Gowar, J.; "Power Mosfets: Theory and Applications," A. Wiley-Interscience Publication © 1989, pp. 5-23. [ISBN 0-471-82867-X].

"Power Mosfet Technology," Lidow et al., (International Electron Devices meeting, Dec. 3-5, 1979, *IEAM Technical Digest*, pp. 79-83.

"Optimization of Nonplanar Power MOS Transistors," Lisiak et al., *IEEE Transactions of Electron Devices*, vol. ED-25, No. 10, Oct. 1975, pp. 1229-1234.

\* cited by examiner



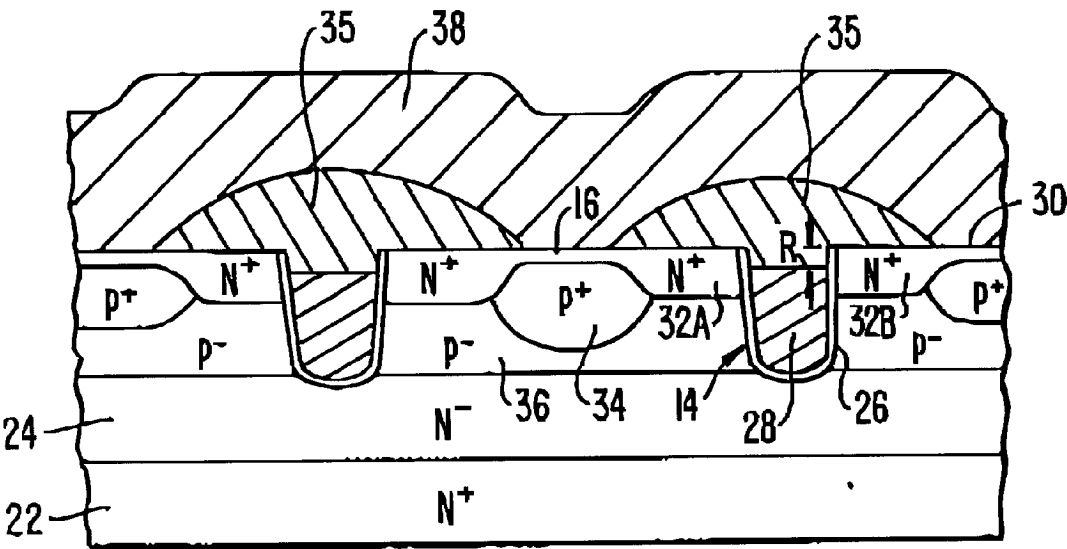


FIG. 1A.

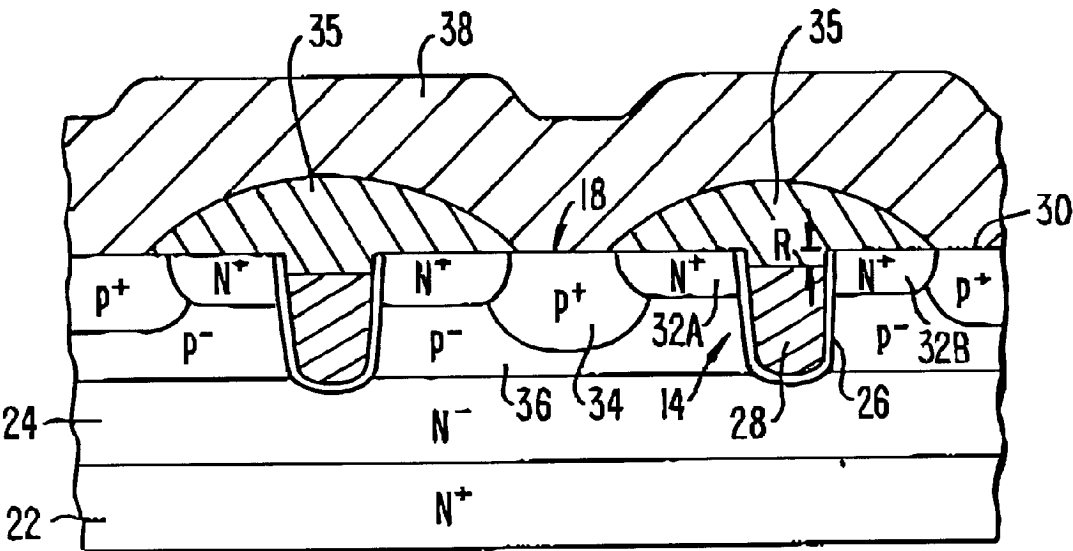
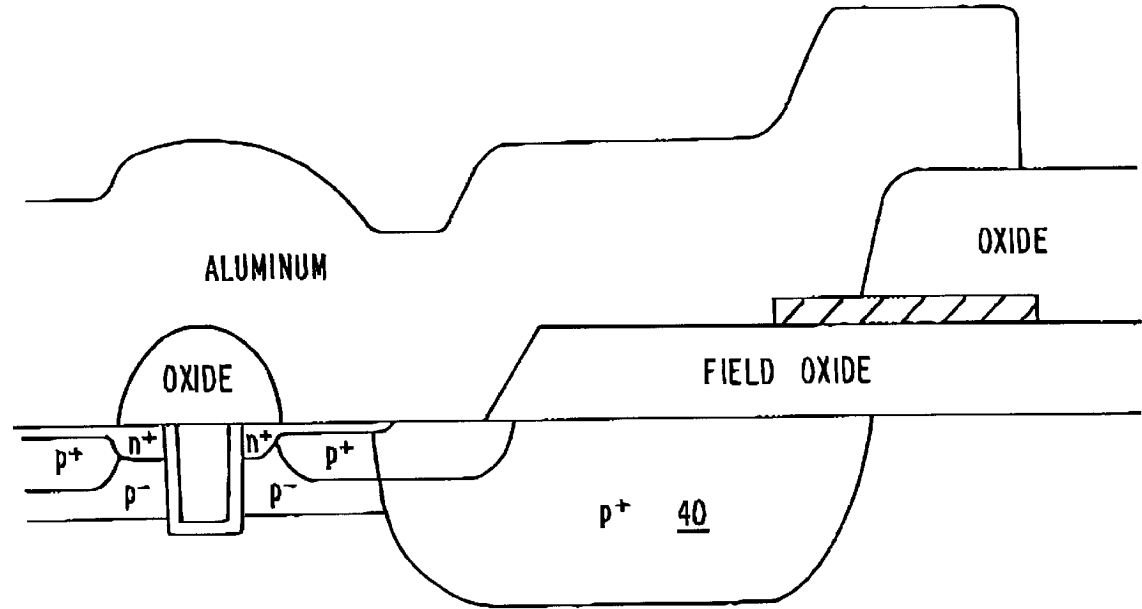


FIG. 1B.



*FIG. 2.*

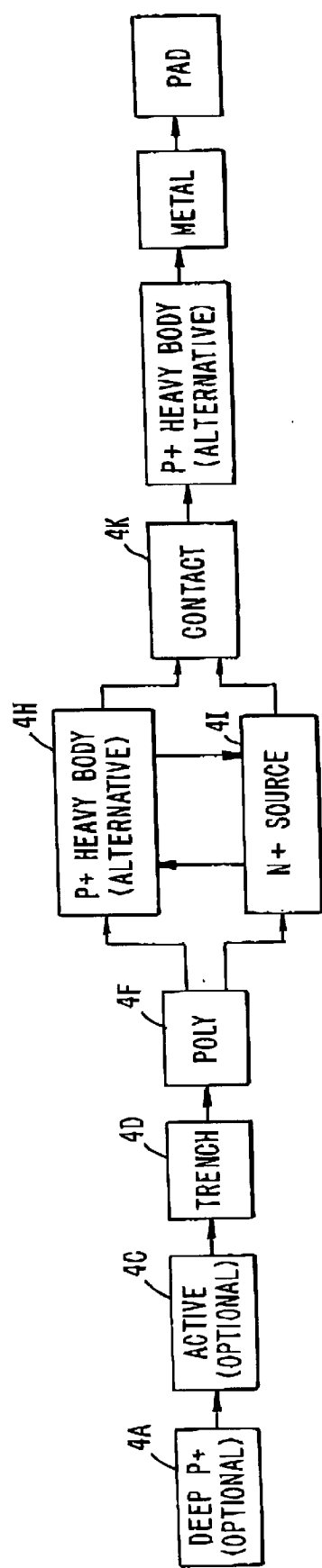


FIG. 3.



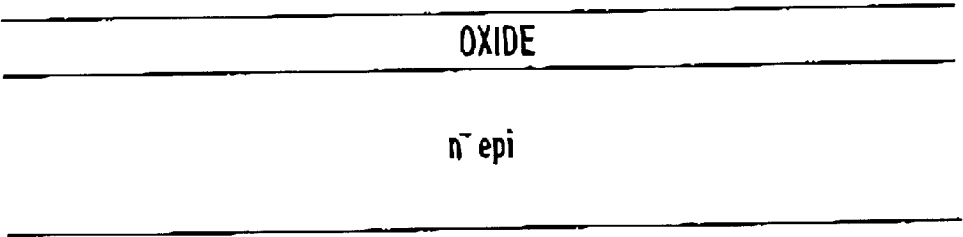


FIG. 4.

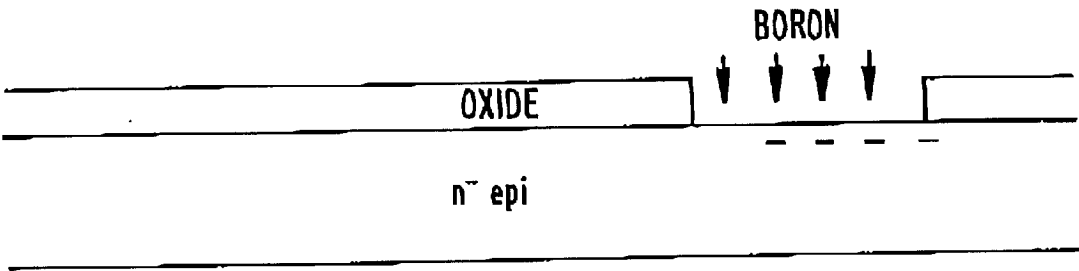


FIG. 4A.

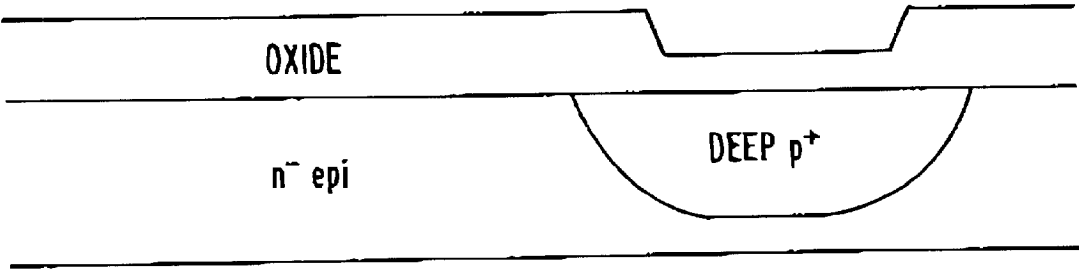


FIG. 4B.

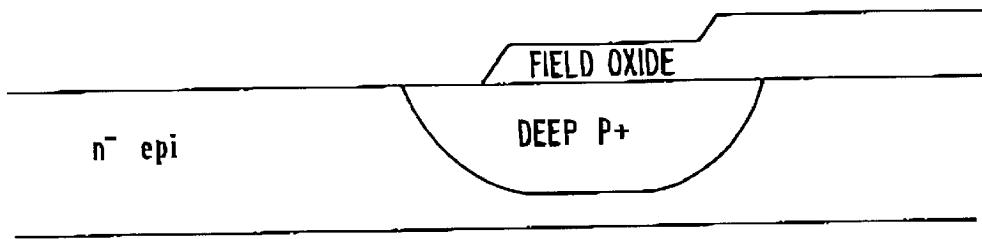


FIG. 4C.

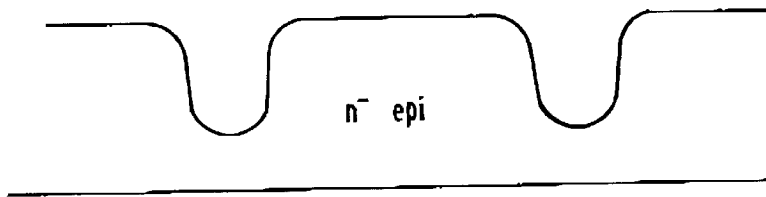


FIG. 4D.

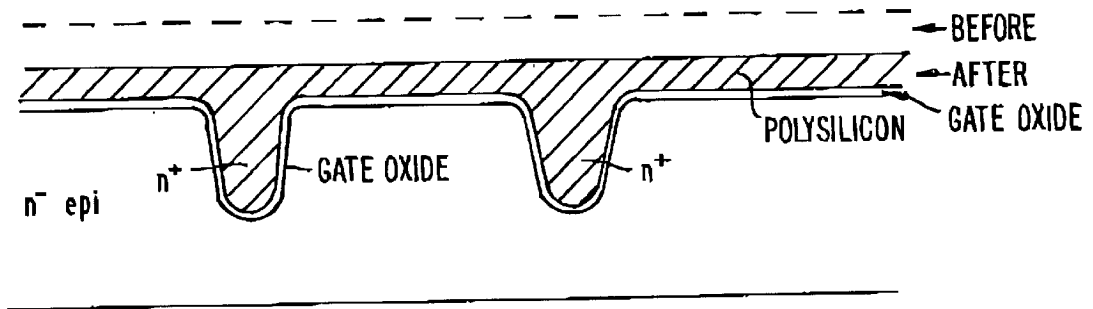


FIG. 4E.

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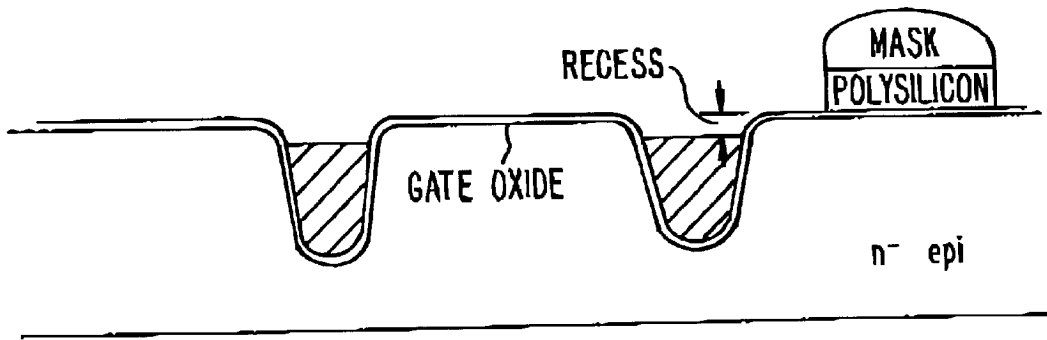


FIG. 4F.

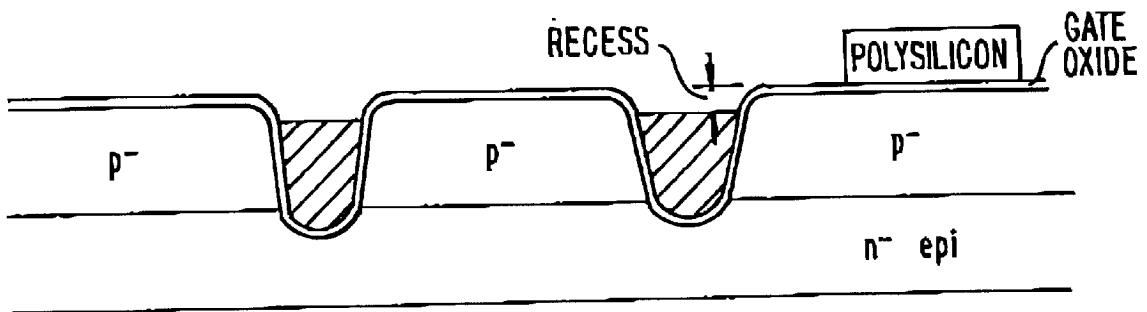


FIG. 4G.

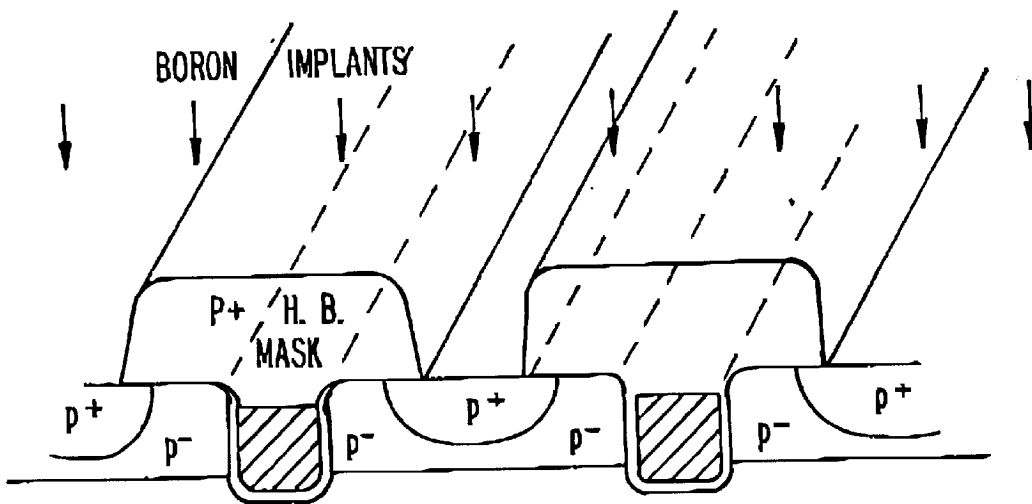


FIG. 4H.

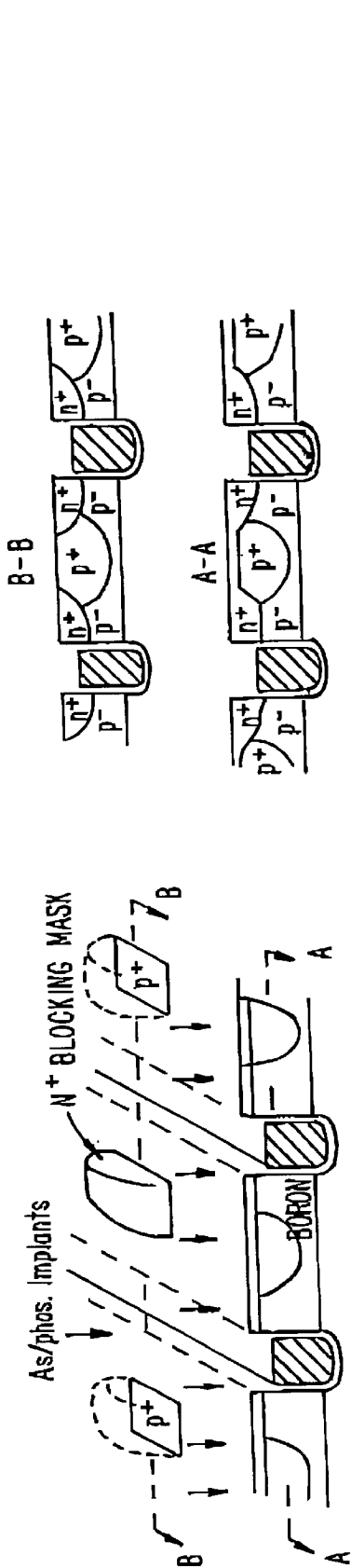


FIG. 4I.

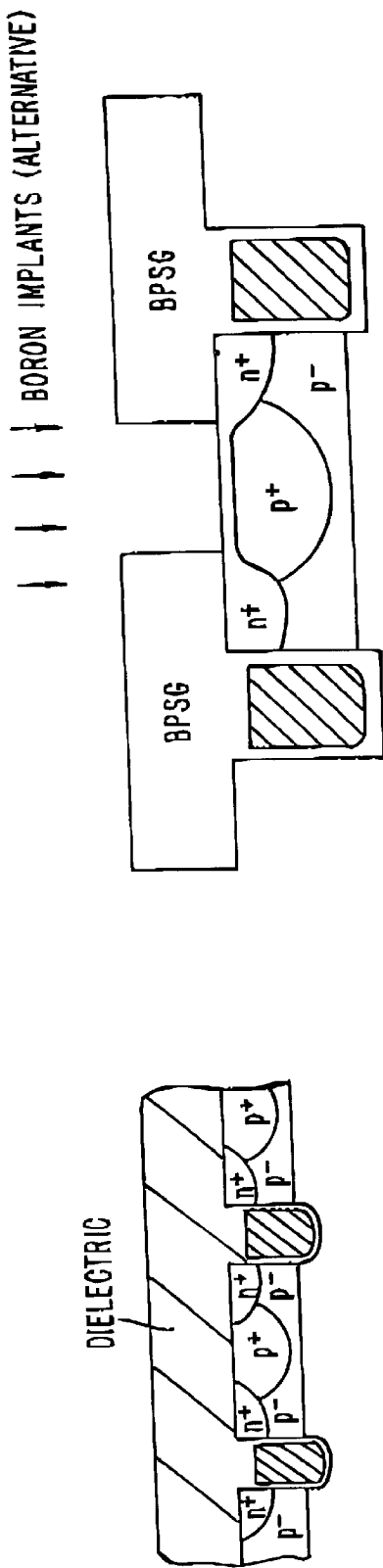


FIG. 4J.

FIG. 4K.

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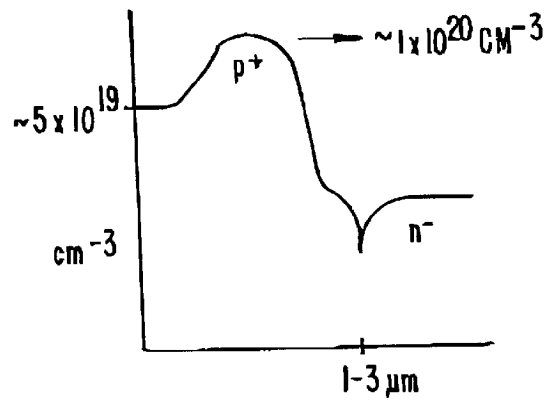


FIG. 5.

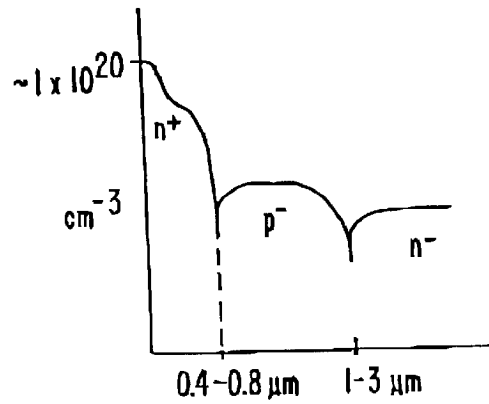


FIG. 5A.

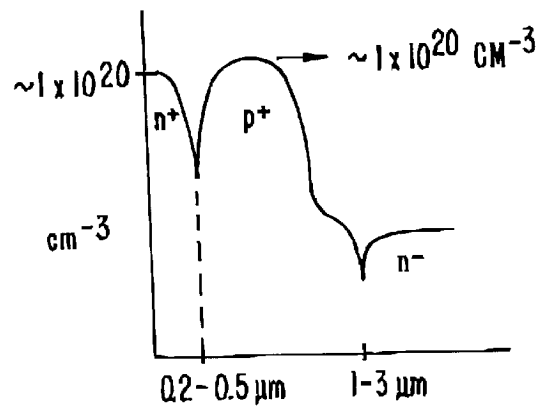


FIG. 5B.

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**FIELD EFFECT TRANSISTOR AND  
METHOD OF ITS MANUFACTURE****BACKGROUND OF THE INVENTION**

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trench DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ( $R_{ds(on)}$ ) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the

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breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

**SUMMARY OF THE INVENTION**

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trench DMOS transistors exhibit low  $R_{ds(on)}$ , low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trench field effect transistor that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped wells have a depth less than the predetermined depth of the trenches. The trenches have rounded top and bottom corners. There is an abrupt junction at the interface between each heavy body and the corresponding well, to cause the peak electric field, when voltage is applied to the transistor, to

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occur in the area of the interface. The array also includes a field termination structure surrounding the periphery of the array. The field termination structure includes a well having a depth greater than that of the gate-forming trenches. The field termination structure includes a termination trench extending continuously around the periphery of the array, more preferably a plurality of concentrically arranged termination trenches.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The field termination structure includes a doped well. The field termination structure includes a termination trench. The field termination structure includes a plurality of concentrically arranged termination trenches. Each of the DMOS transistor cells further comprises a doped heavy body and the doped heavy body extends into the semiconductor substrate to a depth that is less than the predetermined depth of the gate-forming trenches.

The invention also features a method of making a heavy body structure for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about 1E15 to 5E15. The second energy is from about 20 to 40 keV. The second dosage is from about 1E14 to 1E15.

Additionally, the invention features a method of making a source for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about 5E15 to 1E16. The second energy is from about 40 to 70 keV. The second dosage is from about 1E15 to 5E15. The resulting depth of the source is from about 0.4 to 0.8  $\mu\text{m}$  in the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trenched field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type

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to form a plurality of wells interposed between adjacent trenches, (g) patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4-4k are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4-4k are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5 and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trenched DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1a, while the regions that have a p+ contact are shown in FIG. 1b.

As shown in FIGS. 1a and 1b, each trenched DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to 0.4  $\mu\text{m}$ ). N+ doped source regions 32a, 32b are positioned one on each side of the trench 14. A dielectric layer 35 covers the trench opening and the two source regions 32a, 32b. Extending between the source regions of adjacent cells is a p+ heavy body region 34 and, beneath it,



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a flat-bottomed p- well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1a** and **1b** includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p- well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in copending application U.S. Ser. No. 08/959,197, filed on Oct. 28, 1997. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p- well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and draws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3  $\mu\text{m}$  deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4-4k**. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4-4k**. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4-4k** can be varied. Moreover, some of the steps shown in FIGS. **4-4k** are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500  $\mu\text{m}$ , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10  $\mu\text{m}$ . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4-4c**. In FIG. **4**, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4a**, the oxide layer is patterned and etched to

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define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of  $1\text{E}14$  ( $1 \times 10^{14}$ ) to  $1\text{E}16$   $\text{cm}^{-2}$ . As shown in FIG. **4b**, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4-4c**, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4d-4k**. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4d**). Preferably, as noted above, the trenches are formed using the process described in copending application U.S. Ser. No. 08/959, 197, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4e**, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2  $\mu\text{m}$  depending on the trench width (shown by the dotted lines in FIG. **4e**). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 kÅ (indicated by solid lines in FIG. **4e**). The polysilicon is then doped to n-type, e.g., by conventional  $\text{POCL}_3$  doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4f**. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4g**, the p- well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of  $1\text{E}13$  to  $1\text{E}15$ , and driving it in to a depth of from about 1 to 3  $\mu\text{m}$  using conventional drive in techniques.



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The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. 3. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4h. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4k, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1  $\mu\text{m}$  deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5  $\mu\text{m}$  deep), and includes a region of high dopant concentration near the interface with the p- well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1b), as shown in FIG. 4i. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4i, which correspond to FIGS. 1a and 1b).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8  $\mu\text{m}$  after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type surface of the p+

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heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower  $R_{ds, on}$ .

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4j), after which the dielectric is patterned and etched (FIG. 4k) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A trenched field effect transistor comprising:

- a semiconductor substrate having dopants of a first conductivity type;
- a trench extending a predetermined depth into said semiconductor substrate;
- a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;
- a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and
- a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

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2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.

5. The trenched field effect transistor of claim 4 wherein said doped heavy body has a first dopant concentration near the abrupt junction and a second dopant concentration near its upper surface that is less than the first dopant concentration.

6. An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

7. The array of transistor cells of claim 6, wherein each said doped well has a substantially flat bottom.

8. The array of transistor cells of claim 6 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.

9. The array of transistor cells of claim 6 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.

10. The array of transistor cells of claim 6 wherein each said gate-forming trench has rounded top and bottom corners.

11. The array of transistor cells of claim 9 further comprising a field termination structure surrounding the periphery of the array.

12. The array of transistor cells of claim 11 wherein said field termination structure comprises a well having a depth greater than that of the gate-forming trenches.

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13. The array of transistor cells of claim 11 wherein said field termination structure comprises a termination trench extending continuously around the periphery of the array.

14. The array of transistor cells of claim 13 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

15. A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

16. The trenched field effect transistor of claim 15 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.

17. The trenched field effect transistor of claim 16 wherein the contact areas alternate between source and heavy body contacts.

18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

19. The semiconductor die of claim 18 wherein said field termination structure comprises a deep doped well.

20. The trenched field effect transistor of claim 19 wherein said double implant comprises a first high energy implant to reach said second depth, and a second lower energy implant to extend the heavy body from said second depth to substantially a surface of the substrate.

21. The trenched field effect transistor of claim 6, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

22. The trenched field effect transistor of claim 15, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,429,481 B1  
DATED : August 6, 2002  
INVENTOR(S) : Mo et al.

Page 1 of 1

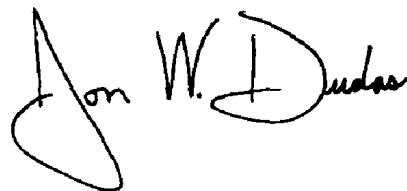
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4,

Line 38, should read -- Figs. 5, 5a and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor. --

Signed and Sealed this

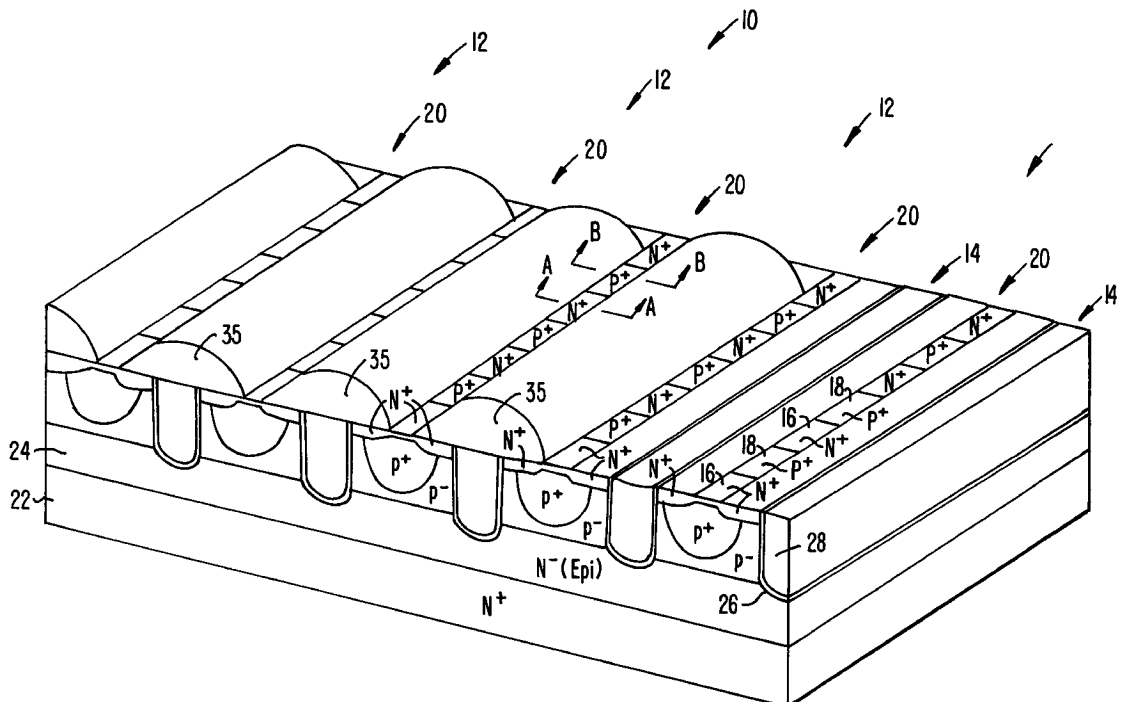
Twenty-fifth Day of May, 2004

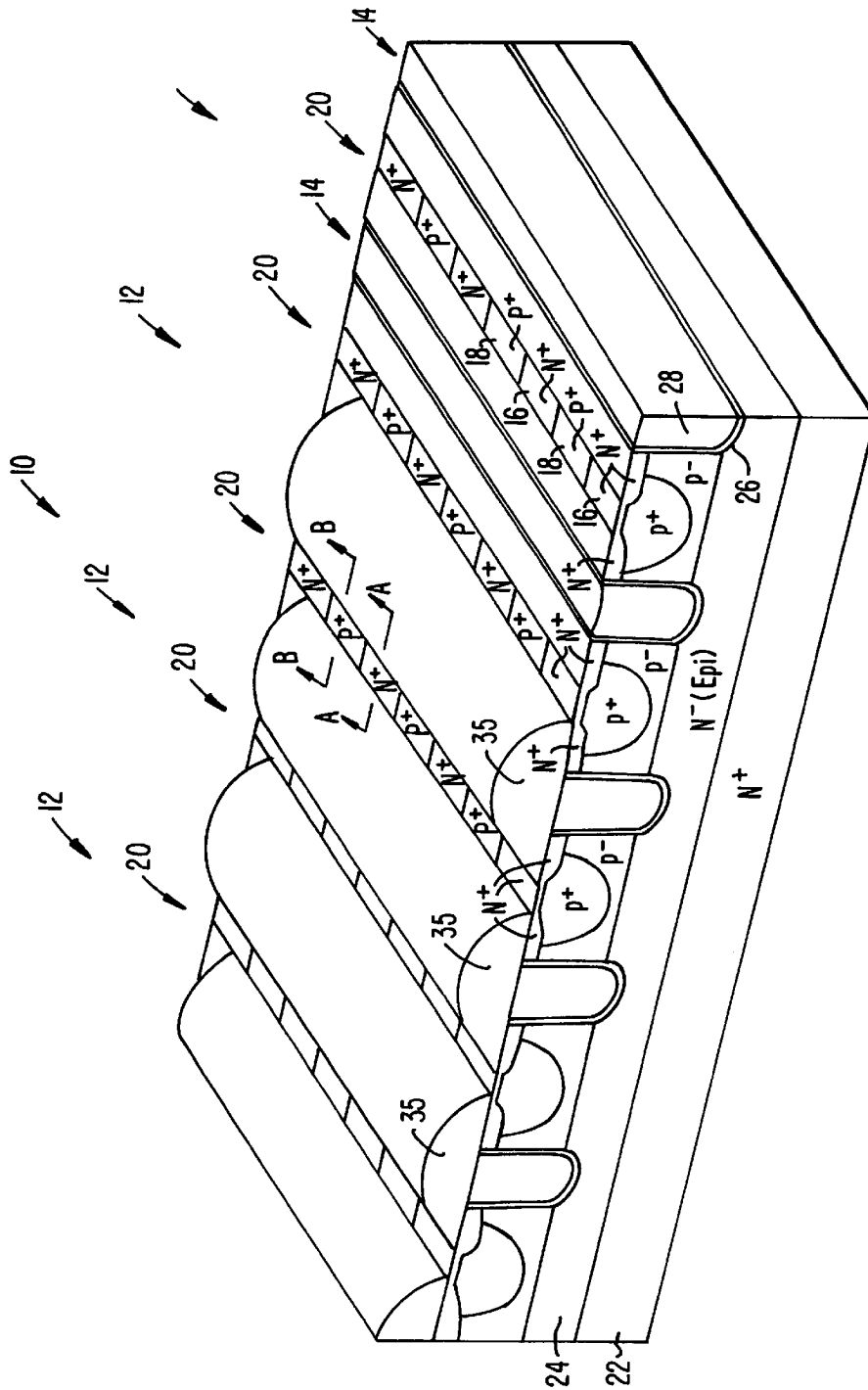
A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large loop for the "J" and a cursive "Dudas".

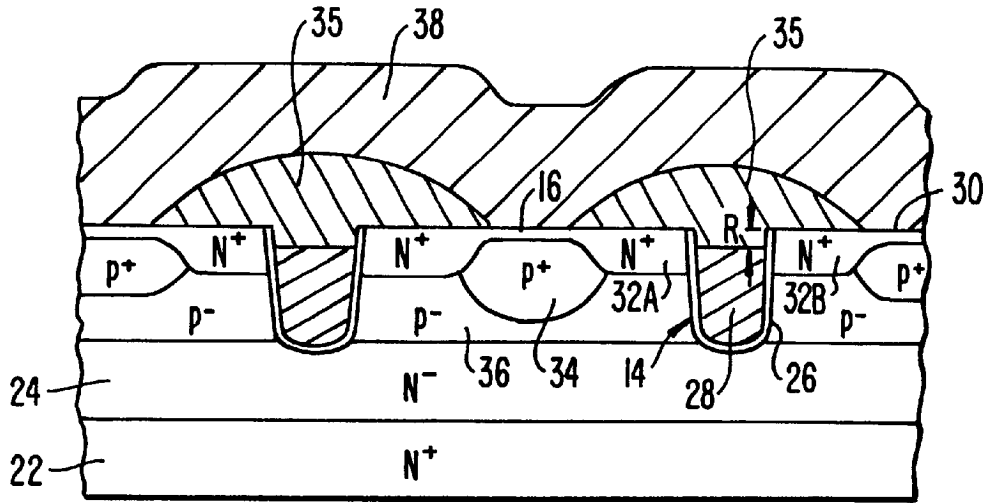
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JON W. DUDAS  
*Acting Director of the United States Patent and Trademark Office*

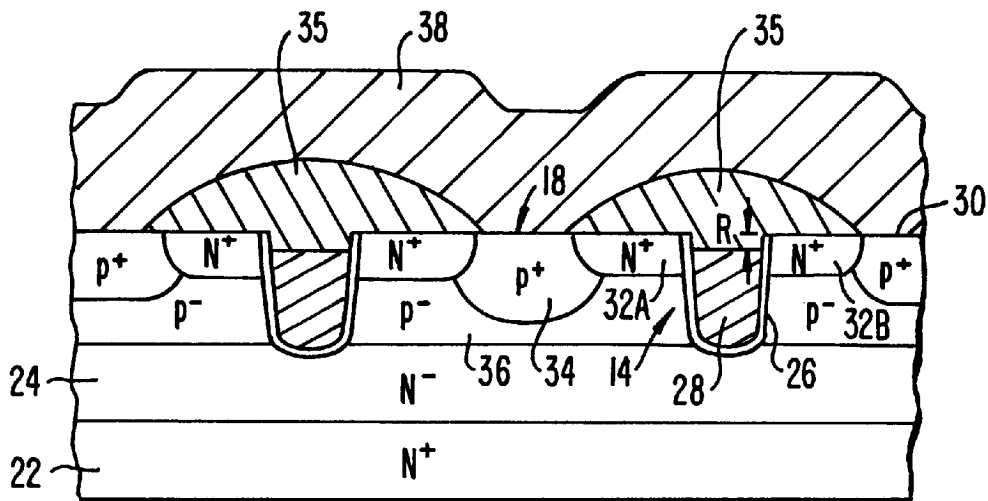
## **EXHIBIT 2**







**FIG. 1A.**



**FIG. 1B.**

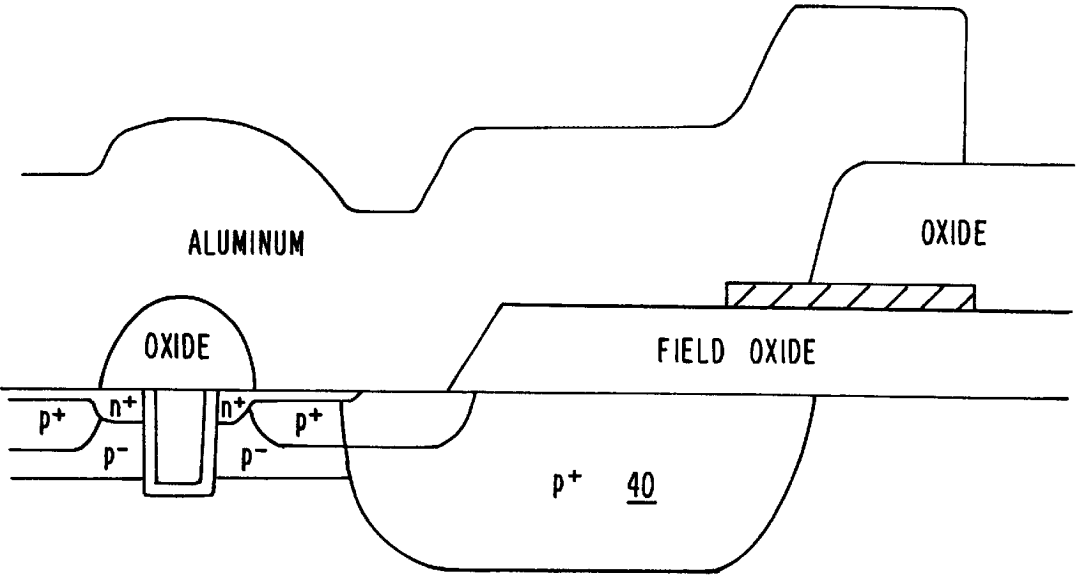


FIG. 2.



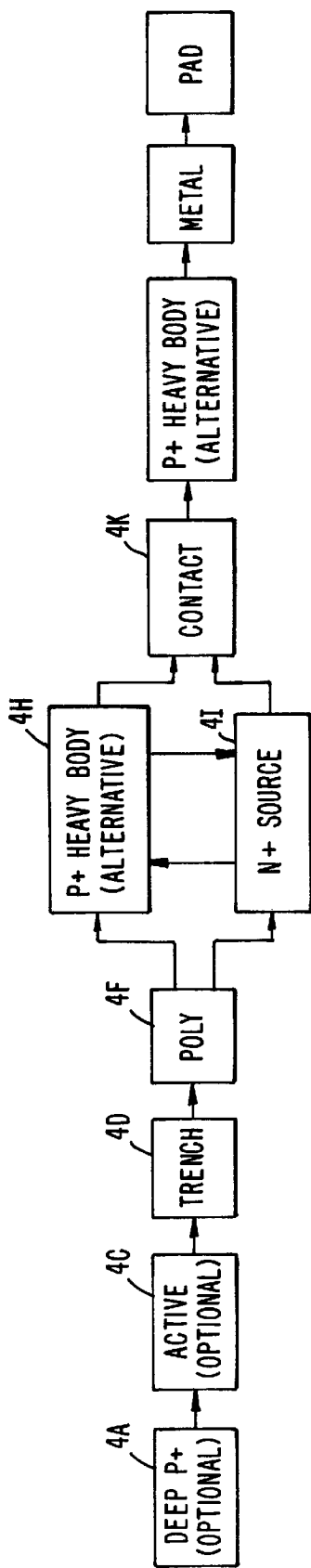


FIG. 3.

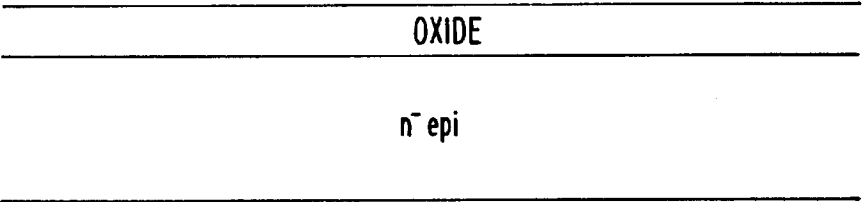


FIG. 4.

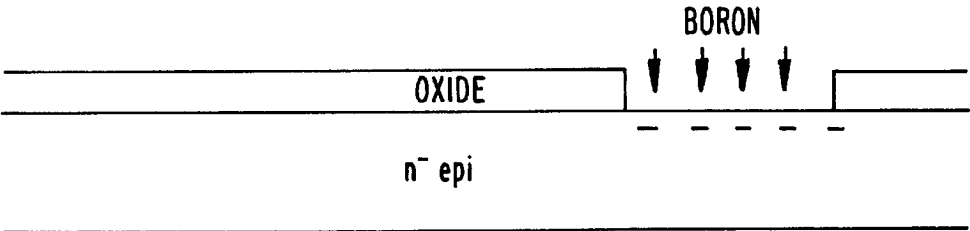


FIG. 4A.

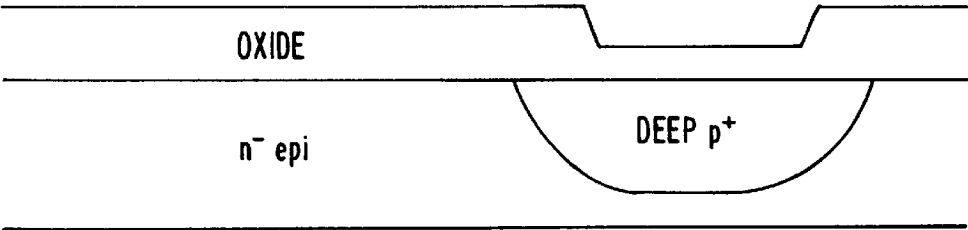


FIG. 4B.

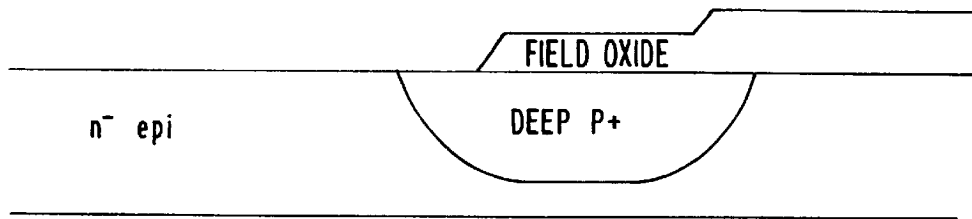


FIG. 4C.

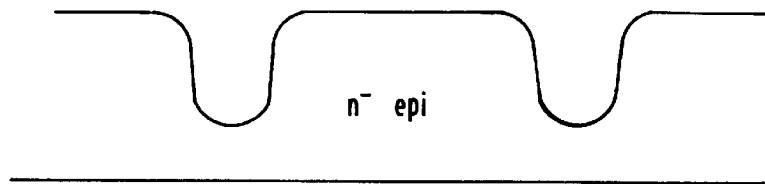


FIG. 4D.

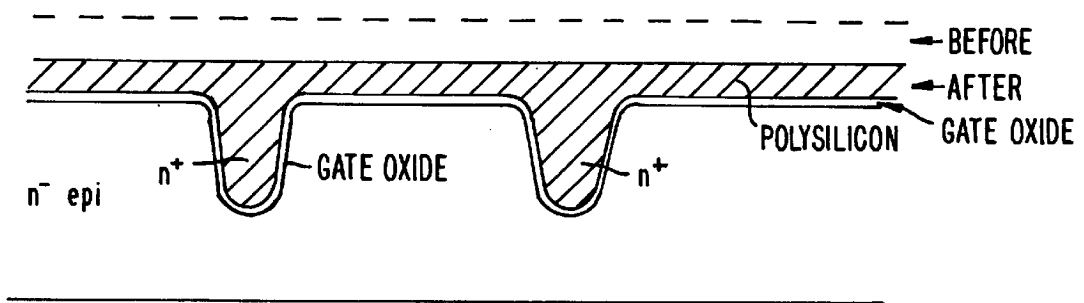


FIG. 4E.

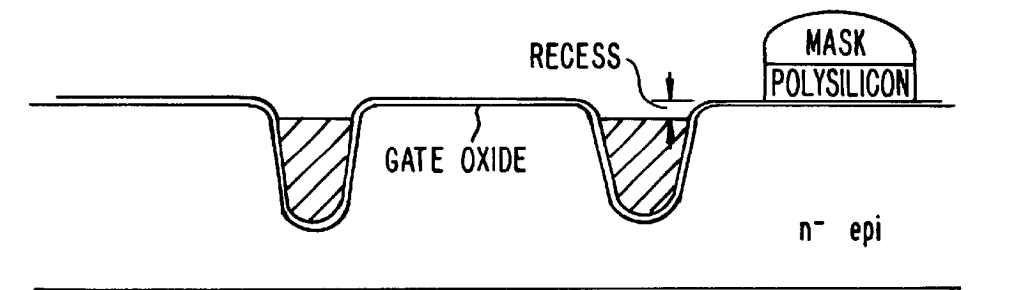


FIG. 4F.

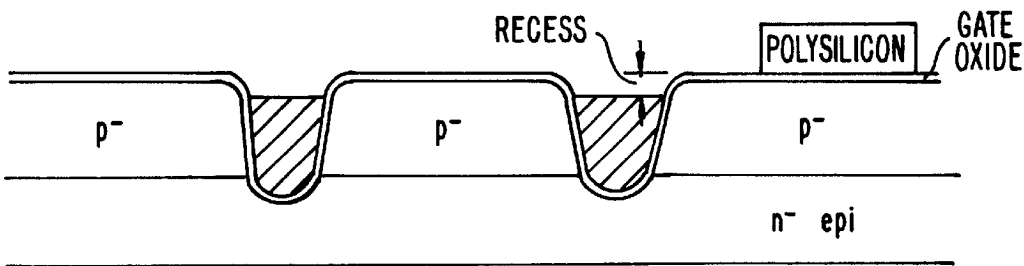


FIG. 4G.

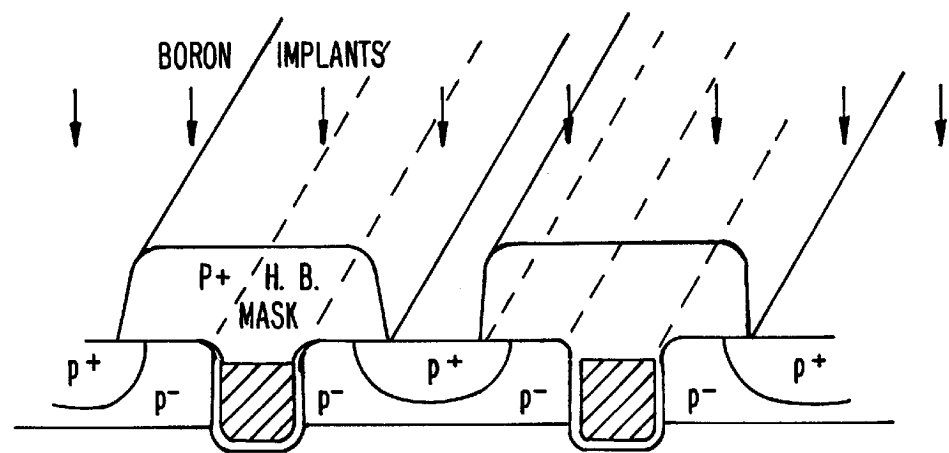


FIG. 4H.

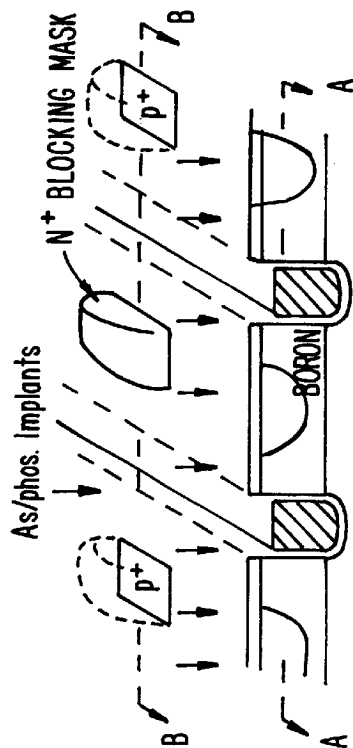


FIG. 4I.

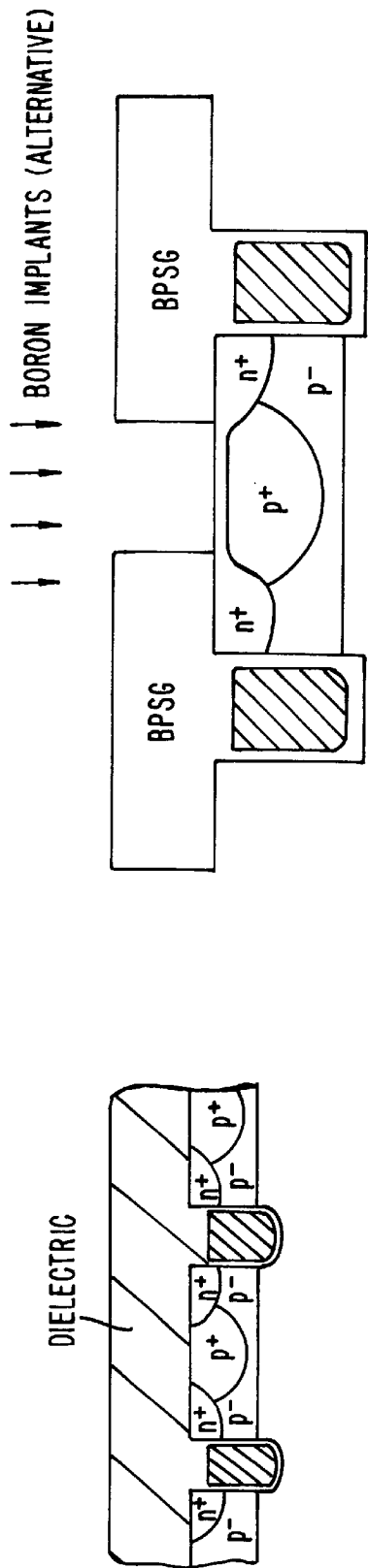


FIG. 4J.

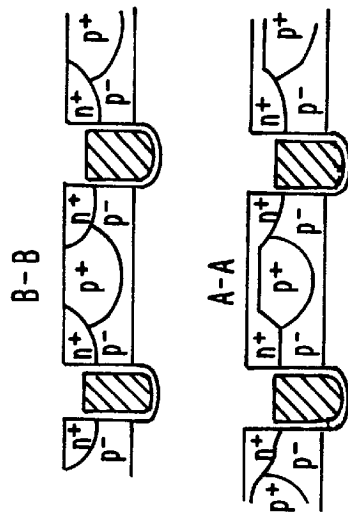


FIG. 4K.

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Feb. 18, 2003

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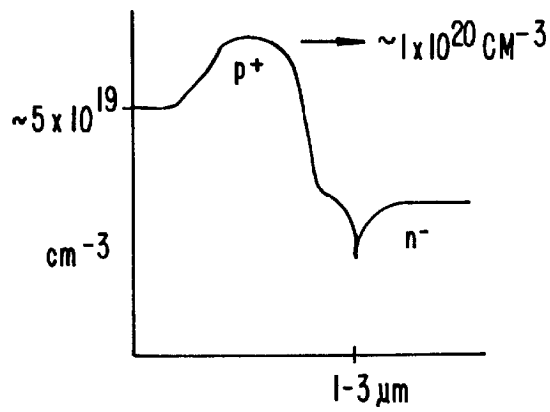


FIG. 5.

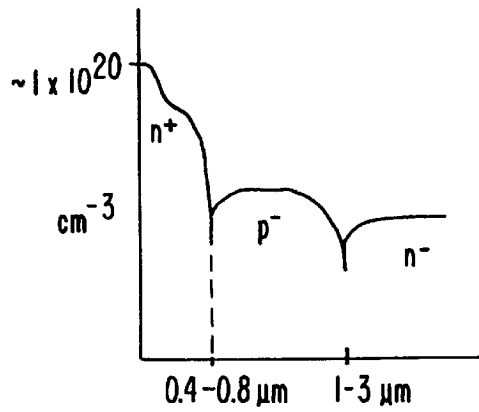


FIG. 5A.

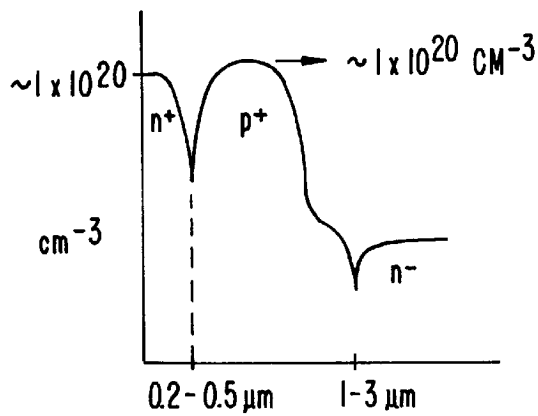


FIG. 5B.

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## METHOD OF MANUFACTURING A FIELD EFFECT TRANSISTOR

This application is a division of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997 now U.S. Pat. No. 6,429,481.

### BACKGROUND OF THE INVENTION

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trench DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ( $R_{ds(on)}$ ) when turned on and low parasitic capacitance. The transistor structure should also avoid "punch through". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field

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termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

### SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trench DMOS transistors exhibit low  $R_{ds(on)}$ , low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trench field effect transistor that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped wells have a depth less than the predetermined depth of the trenches. The trenches have rounded top and bottom corners.

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There is an abrupt junction at the interface between each heavy body and the corresponding well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface. The array also includes a field termination structure surrounding the periphery of the array. The field termination structure includes a well having a depth greater than that of the gate-forming trenches. The field termination structure includes a termination trench extending continuously around the periphery of the array, more preferably a plurality of concentrically arranged termination trenches.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ . The second energy is from about 20 to 40 keV. The second dosage is from about  $1\text{E}14$  to  $1\text{E}15\text{ cm}^{-2}$ .

The invention also features a method of making a heavy body structure for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about  $1\text{E}15$  to  $5\text{E}15$ . The second energy is from about 20 to 40 keV. The second dosage is from about  $1\text{E}14$  to  $1\text{E}15$ .

Additionally, the invention features a method of making a source for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about  $5\text{E}15$  to  $1\text{E}16\text{ cm}^{-2}$ . The second energy is from about 40 to 70 keV. The second dosage is from about  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ . The resulting depth of the source is from about 0.4 to  $0.8\text{ }\mu\text{m}$  the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trench field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type

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to form a plurality of wells interposed between adjacent trenches, (g) patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4-4k are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4-4k are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5 and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trench DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1a, while the regions that have a p+ contact are shown in FIG. 1b.

As shown in FIGS. 1a and 1b, each trench DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to  $0.4\text{ }\mu\text{m}$ ). N+ doped source regions 32a, 32b are positioned one on each side of the trench 14. A dielectric layer 35 covers the trench opening and the two source regions 32a, 32b. Extending between the source regions of adjacent cells is a p+ heavy body region 34 and, beneath it,



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a flat-bottomed p- well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1a** and **1b** includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p- well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in copending application U.S. Ser. No. 08/959,197, filed on Oct. 28, 1997. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p- well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and thaws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3  $\mu\text{m}$  deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4-4k**. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4-4k**. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4-4k** can be varied. Moreover, some of the steps shown in FIGS. **4-4k** are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500  $\mu\text{m}$ , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10  $\mu\text{m}$ . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4-4c**. FIG. **4**, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4a**, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well

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field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of  $1\text{E}14$  ( $1 \times 10^{14}$ ) to  $1\text{E}16$   $\text{cm}^{-2}$ . As shown in FIG. **4b**, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4-4c**, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4d-4k**. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4d**). Preferably, as noted above, the trenches are formed using the process described in copending application U.S. Pat. No. 08/959, 197, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4e**, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2  $\mu\text{m}$  depending on the trench width (shown by the dotted lines in FIG. **4e**). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 k Å (indicated by solid lines in FIG. **4e**). The polysilicon is then doped to n-type, e.g., by conventional  $\text{POCl}_3$  doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4f**. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4g**, the p- well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of  $1\text{E}13$  to  $1\text{E}15$ , and driving it in to a depth of from about 1 to 3  $\mu\text{m}$  using conventional drive in techniques.

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The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. 3. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4h. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4k, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ , and a second boron implant at an energy of 20 to 40 keV and a dose of  $1\text{E}14$  to  $1\text{E}15\text{ cm}^{-2}$ . The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1  $\mu\text{m}$  deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5  $\mu\text{m}$  deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1b), as shown in FIG. 4i. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4l, which correspond to FIGS. 1a and 1b).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of  $5\text{E}15$  to  $1\text{E}16\text{ cm}^{-2}$  followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ . The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8  $\mu\text{m}$  after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type

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surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower  $R_{ds,on}$ .

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4j), after which the dielectric is patterned and etched (FIG. 4k) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "if" doped instead, and vice versa.

What is claimed is:

1. A method of making a heavy body structure for a trench DMOS transistor comprising:

providing a semiconductor substrate;

forming a plurality of trenches into the substrate;

implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;

implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body; and

implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body,

wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration that is greater than said dosage of said third dopant.

2. The method of claim 1 wherein said first and second dopants both comprise boron.

3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.

4. The method of claim 3 wherein said first dosage is from about  $1\text{E}13$  to  $1\text{E}15\text{ cm}^{-2}$ .

5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.

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6. The method of claim 5 wherein said second dosage is from about  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ .

7. A method of manufacturing a trench field effect transistor comprising:

forming an epitaxial layer on a semiconductor substrate; 5  
patterning and etching a plurality of trenches into the epitaxial layer;

lining each trench with a gate dielectric layer;

depositing polysilicon to fill the dielectric-lined trenches; 10

doping the polysilicon with a dopant of a first type;

patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches; 15

patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells; 20

patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and

applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, 25

wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively. 30

8. The method of manufacturing a trench field effect transistor of claim 7 wherein the trenches are patterned to extend in one direction and be substantially parallel to each other. 35

9. The method of manufacturing a trench field effect transistor of claim 7 wherein the patterning and implanting steps further comprise arranging the first dopant type contact

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areas and second dopant type contact areas in alternation and extend linearly between adjacent trenches.

10. The method of manufacturing a trench field effect transistor of claim 7 wherein the implanting step for forming the source regions comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, the second energy and dosage being less than the first energy and dosage, respectively.

11. The method of manufacturing a trench field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.

12. The method of manufacturing a trench field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies. 15

13. The method of manufacturing a trench field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.

14. The method of manufacturing a trench field effect transistor of claim 13 wherein said field termination structure is formed by forming a deep well doped with a dopant of the second dopant type. 20

15. The method of manufacturing a trench field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts. 25

16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about  $1\text{E}14$  to  $1\text{E}15\text{ cm}^{-2}$ . 30

17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.

18. The method of manufacturing a trench field effect transistor of claim 13 wherein said field terminations structure is formed by forming a trench ring. 35

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,521,497 B2  
DATED : February 18, 2003  
INVENTOR(S) : Mo

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4,

Line 38, should read:

-- Figs. 5, 5a and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor. --

Signed and Sealed this

Twenty-fourth Day of February, 2004

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large loop for the "J" and a cursive "Dudas".

JON W. DUDAS

*Acting Director of the United States Patent and Trademark Office*

## **EXHIBIT 3**

(12) **United States Patent**  
**Mo et al.**

(10) **Patent No.:** **US 6,710,406 B2**  
(45) **Date of Patent:** **\*Mar. 23, 2004**

(54) **FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean Edward Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 35 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/155,554**

(22) Filed: **May 24, 2002**

(65) **Prior Publication Data**

US 2002/0140027 A1 Oct. 3, 2002

**Related U.S. Application Data**

(63) Continuation of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 29/78**

(52) **U.S. Cl.** ..... **257/341; 257/331**

(58) **Field of Search** ..... **257/331, 341**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,070,690 A	1/1978	Wickstrom
4,132,998 A	1/1979	Dingwall
4,145,703 A	3/1979	Blanchard et al.
4,326,332 A	4/1982	Kenney
4,329,705 A	5/1982	Baker
4,344,081 A	8/1982	Pao et al.
4,345,265 A	8/1982	Blanchard

4,398,339 A	8/1983	Blanchard et al.
4,503,449 A	3/1985	David et al.
4,503,598 A	3/1985	Vora et al.
4,541,001 A	9/1985	Schutten et al.

(List continued on next page.)

**FOREIGN PATENT DOCUMENTS**

CN	1090680 A	4/1994
EP	0 238 749 A2	9/1987
EP	0 550 770 B1	7/1993

(List continued on next page.)

**OTHER PUBLICATIONS**

Blanchard, R.A., "Optimization of discrete high power MOS transistors," *Stanford Electronics Laboratory, Integrated Circuits Laboratory*, Apr. 1982, Technical Report No. IDEZ696-2.

Chang, T.S. and Critchlow, D.L., "Verticle FET random-access memories with deep trench isolation," *IBM Technical Disclosure Bulletin*, Jan. 1980, pp. 3683-3687, vol. 22(8B).  
Grant, D.A. and Gower, J., "The development of power MOS devices," Chapter 1.2 *In Power Mosfets: Theory and applications*. John Wiley & Sons; New York, 1989, pp. 5-23.

(List continued on next page.)

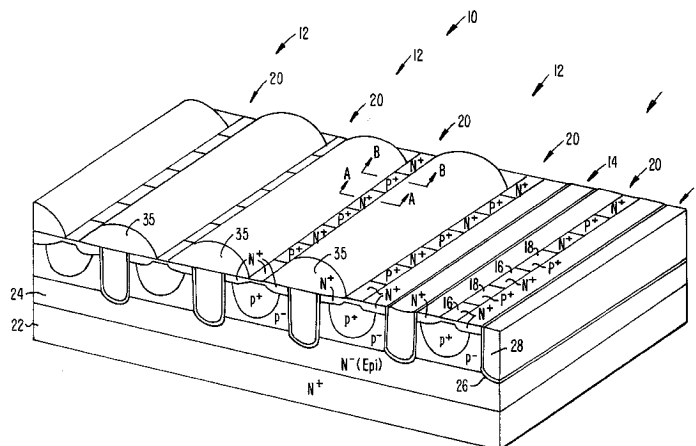
*Primary Examiner*—Jerome Jackson

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(57) **ABSTRACT**

A trench field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

**32 Claims, 9 Drawing Sheets**





## US 6,710,406 B2

Page 2

## U.S. PATENT DOCUMENTS

4,639,762 A 1/1987 Neilson et al.  
 4,682,405 A 7/1987 Blanchard et al.  
 4,683,643 A 8/1987 Nakajima et al.  
 4,767,722 A 8/1988 Blanchard  
 4,808,543 A 2/1989 Parrillo et al.  
 4,845,537 A 7/1989 Nishimura et al.  
 4,860,072 A 8/1989 Zommer  
 4,881,105 A 11/1989 Davari et al.  
 4,893,160 A 1/1990 Blanchard  
 4,914,058 A 4/1990 Blanchard  
 4,967,245 A 10/1990 Cogan et al.  
 4,983,535 A 1/1991 Blanchard  
 5,016,068 A 5/1991 Mori  
 5,017,504 A 5/1991 Nishimura et al.  
 5,045,900 A 9/1991 Tamagawa  
 5,072,266 A 12/1991 Bulucea et al.  
 5,124,764 A 6/1992 Mori  
 5,160,491 A 11/1992 Mori  
 5,168,331 A 12/1992 Yilmaz  
 5,298,442 A 3/1994 Bulucea et al.  
 5,298,780 A 3/1994 Harada  
 5,316,959 A 5/1994 Kwan et al.  
 5,321,289 A 6/1994 Baba et al.  
 5,341,011 A 8/1994 Hshieh et al.  
 5,405,794 A 4/1995 Kim  
 5,410,170 A 4/1995 Bulucea et al.  
 5,430,324 A 7/1995 Bencuya  
 5,455,190 A 10/1995 Hsu  
 5,460,985 A 10/1995 Tokura et al.  
 5,468,982 A 11/1995 Hshieh et al.  
 5,474,943 A 12/1995 Hshieh et al.  
 5,508,534 A 4/1996 Nakamura et al.  
 5,532,179 A 7/1996 Chang et al.  
 5,541,425 A 7/1996 Nishihara  
 5,558,313 A 9/1996 Hshieh et al.  
 5,567,634 A 10/1996 Hébert et al.  
 5,578,851 A 11/1996 Hshieh et al.  
 5,592,005 A 1/1997 Floyd et al.  
 5,597,765 A 1/1997 Yilmaz et al.  
 5,602,046 A 2/1997 Calafut et al.  
 5,605,852 A 2/1997 Bencuya  
 5,614,751 A 3/1997 Yilmaz et al.  
 5,629,543 A 5/1997 Hshieh et al.  
 5,639,676 A 6/1997 Hshieh et al.  
 5,648,670 A 7/1997 Blanchard  
 5,661,322 A 8/1997 Williams et al.  
 5,665,619 A 9/1997 Kwan et al.  
 5,665,996 A 9/1997 Williams et al.  
 5,674,766 A 10/1997 Darwish et al.  
 5,688,725 A 11/1997 Darwish et al.  
 5,689,128 A 11/1997 Hshieh et al.  
 5,701,026 A 12/1997 Fujishima et al.  
 5,767,550 A 6/1998 Calafut et al.  
 5,776,812 A 7/1998 Takahashi et al.  
 5,780,324 A 7/1998 Tokura et al.  
 5,783,491 A 7/1998 Nakamura et al.  
 5,783,915 A 7/1998 Shida et al.  
 5,801,408 A 9/1998 Takahashi  
 5,814,858 A 9/1998 Williams  
 5,879,971 A 3/1999 Witek  
 5,895,952 A 4/1999 Darwish et al.  
 5,930,630 A 7/1999 Hshieh et al.  
 5,986,304 A 11/1999 Hshieh et al.  
 5,998,836 A 12/1999 Williams  
 5,998,837 A 12/1999 Williams  
 6,015,737 A 1/2000 Tokura et al.  
 6,049,108 A 4/2000 Williams et al.  
 6,204,533 B1 3/2001 Williams et al.

## FOREIGN PATENT DOCUMENTS

EP 0 583 028 A1 2/1994  
 EP 0 698 919 A2 2/1996  
 EP 0 720 235 A2 7/1996  
 EP 0 720 236 A2 7/1996  
 EP 0 746 030 A3 12/1996  
 EP 0 746 030 A2 12/1996  
 EP 0 755 076 A2 1/1997  
 EP 0 795 911 A2 9/1997  
 EP 0 801 425 A1 10/1997  
 GB 2269050 A 1/1994  
 JP 56131960 A 10/1981  
 JP 57018365 A 1/1982  
 JP 57153469 A 9/1982  
 JP 58137254 A 8/1983  
 JP 58210678 A 12/1983  
 JP 59080970 A 5/1984  
 JP 59193064 A 11/1984  
 JP 60028271 A 2/1985  
 JP 61102782 A 5/1986  
 JP 62012167 A 1/1987  
 JP 62016572 A 1/1987  
 JP 62023171 A 1/1987  
 JP 62046569 A 2/1987  
 JP 63114173 A 5/1988  
 JP 05226661 A 9/1993  
 JP 08204194 A 8/1996  
 JP 08250731 A 9/1996  
 JP 08316479 A 11/1996  
 JP 09036362 A 2/1997  
 JP 09102607 A 4/1997  
 JP 09270512 A 10/1997  
 WO 93/03502 A1 2/1993  
 WO 95/34094 A1 12/1995  
 WO 97/07547 A1 2/1997  
 WO 97/16853 A1 5/1997

## OTHER PUBLICATIONS

Goodenough, F., "Dense MOSFET enables portable power control," *Electronic Design* Apr. 14, 1997, pp. 45–50.

Holmes, F.E., and Salama, C.A.T., "V groove M.O.S. transistor technology," *Electronic Letters*, Sep. 20, 1973, pp. 457–458, vol. 9(19).

Holmes, F.E., and Salama, C.A.T., "VMOS—A new MOS integrated circuit technology," *Solid State Electronics* 1974, pp. 791–797, vol. 17.

Lidow, A. et al., "Power Mosfet technology," *IEEE Technical Digest—Int. Electron Devices Meet.* 1979, pp. 79–83.

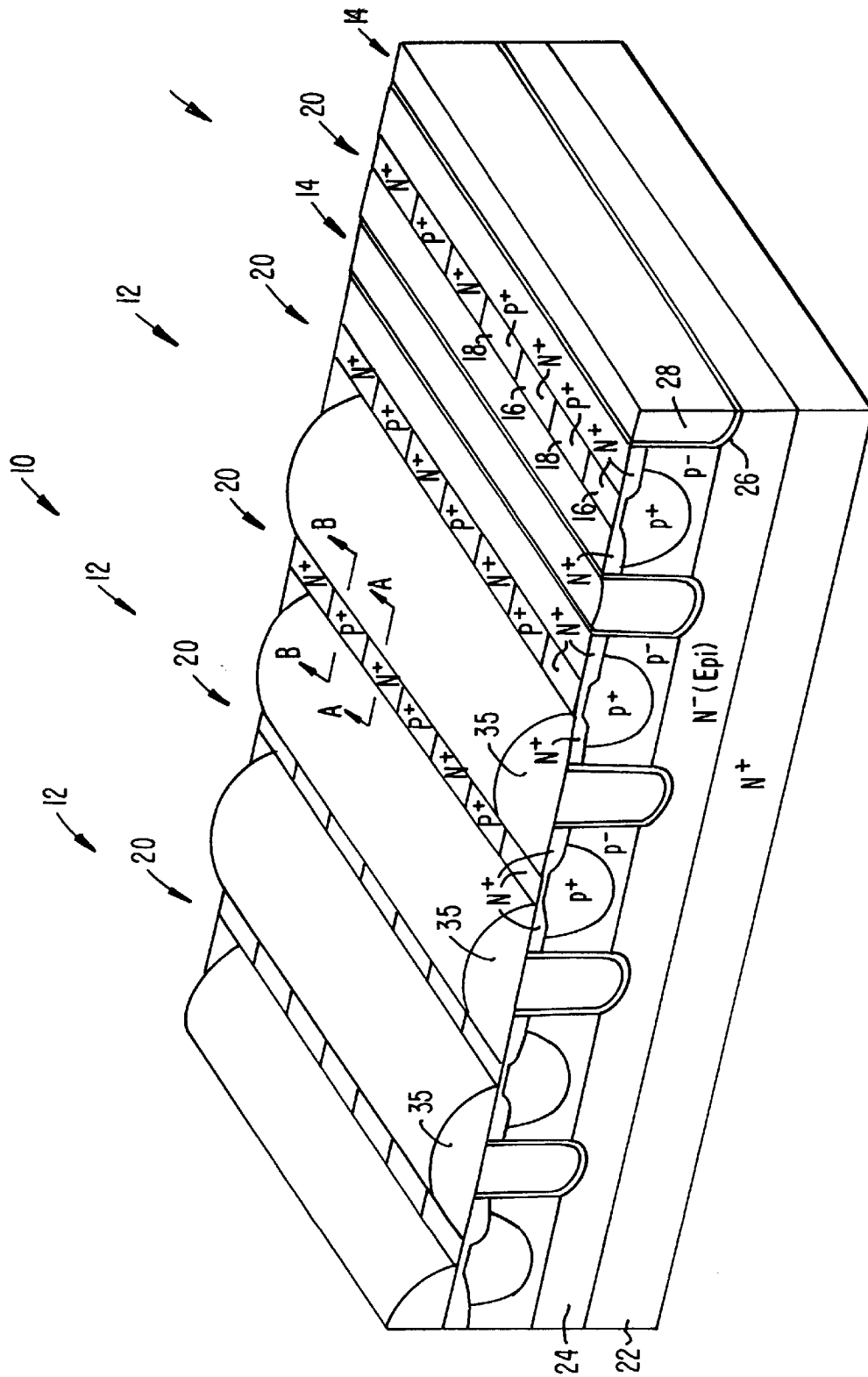
Lisiak, K.P. and Berger, J., "Optimization of nonplanar power MOS transistors," *IEEE Transactions on Electron Devices*, Oct. 1978, pp. 1229–1234, vol. Ed–25(10).

Ou–Yang, P., "Double ion implanted V–MOS technology," *IEEE Journal of Solid–State Circuits*, Feb. 1977, pp. 3–10, vol. SC–12(1).

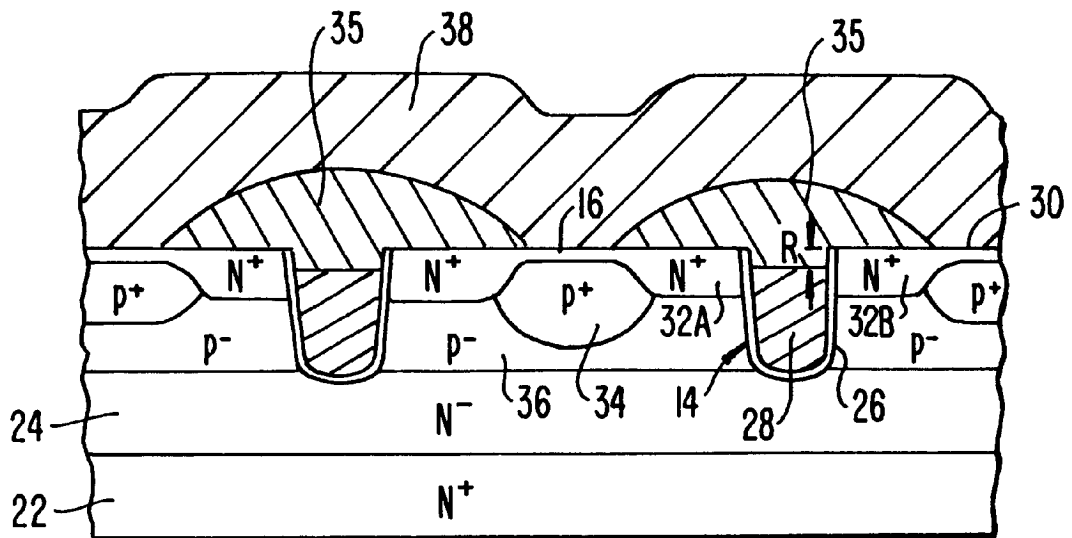
Salama, C.A. and Oakes, J.G., "Nonplanar power field–effect transistors," *IEEE Transactions on Electron Devices*, Oct. 1978, pp. 1222–1228, vol. Ed–25(10).

Sun, S.C., "Physics and technology of power MOSFETs," *Stanford Electronics Laboratory, Integrated Circuits Laboratory*, Feb. 1982, Technical Report No. IDEZ696–1.

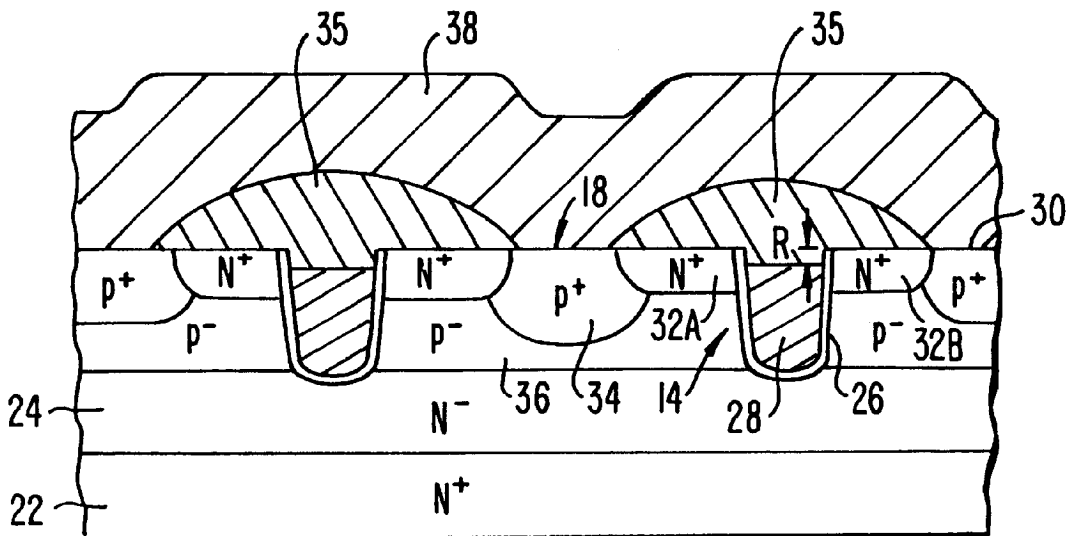
Sze, S.M., "P–N– Junction diode," Chapter 2 *In Physics of Semiconductor Devices*. Second Edition, John Wiley & Sons; New York, 1981, pp. 63–108.







**FIG. 1A.**



**FIG. 1B.**

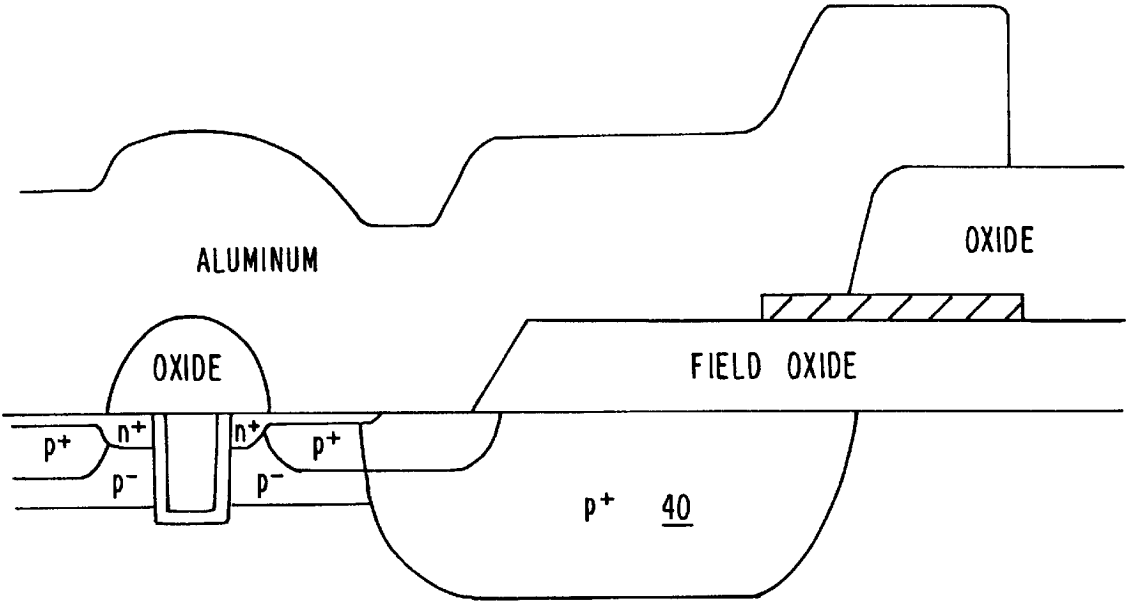


FIG. 2.

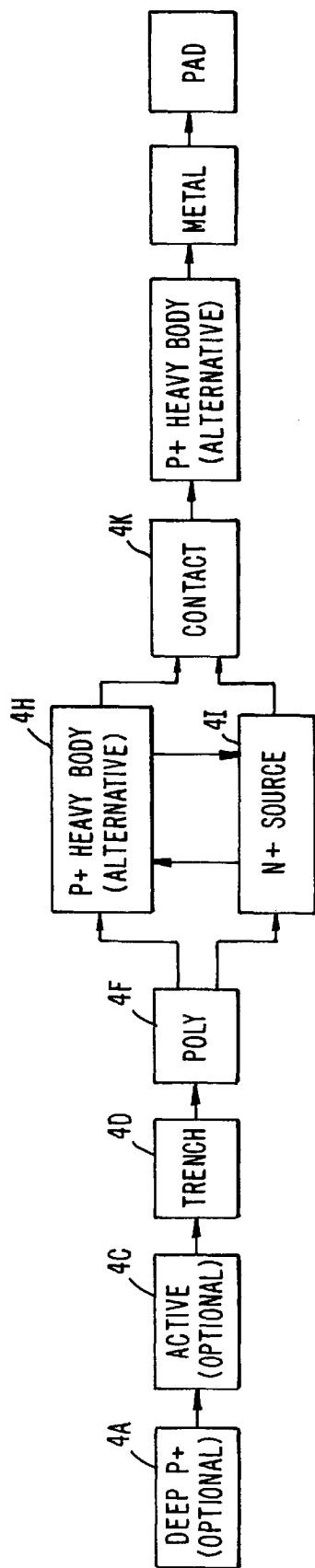


FIG. 3.

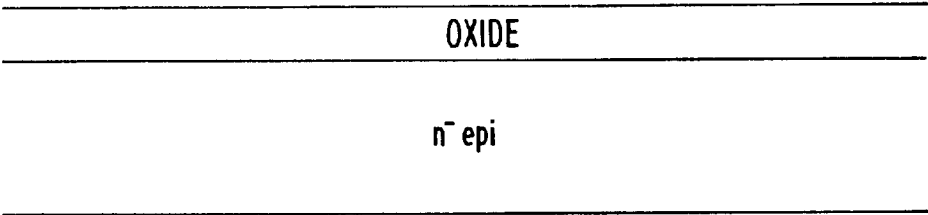


FIG. 4.

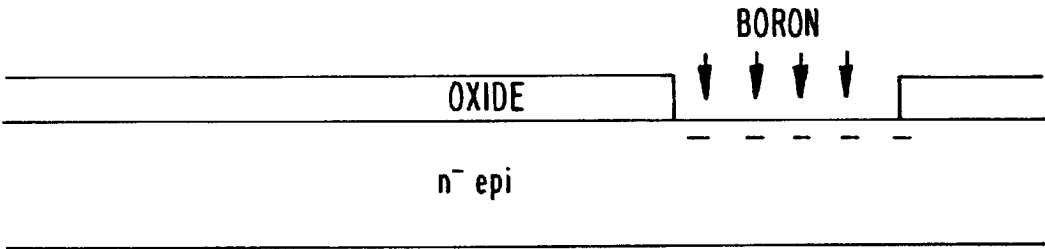


FIG. 4A.

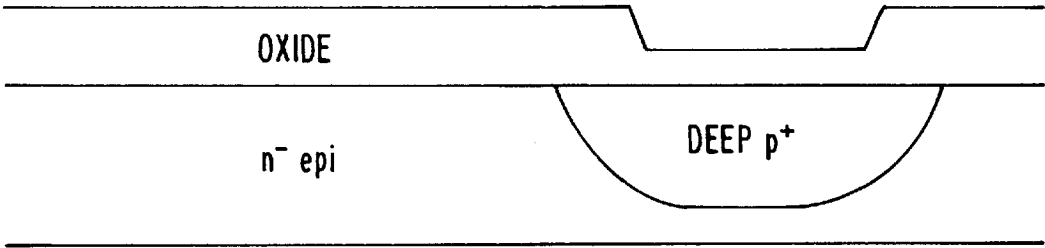


FIG. 4B.

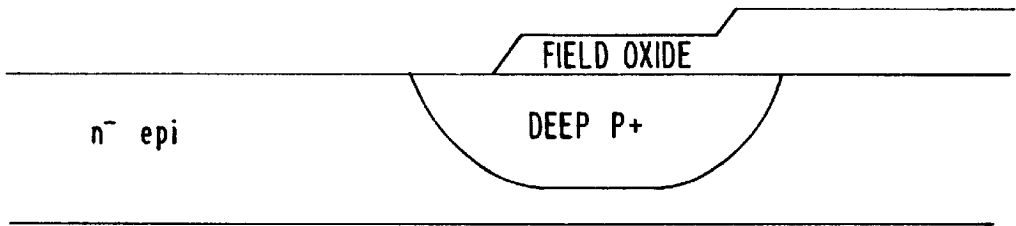


FIG. 4C.

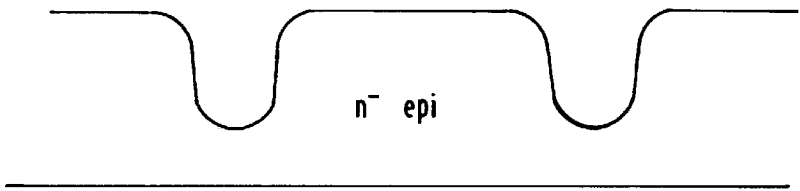


FIG. 4D.

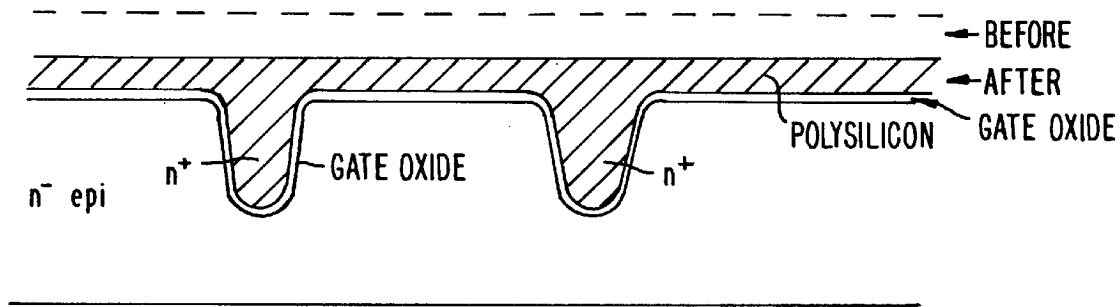


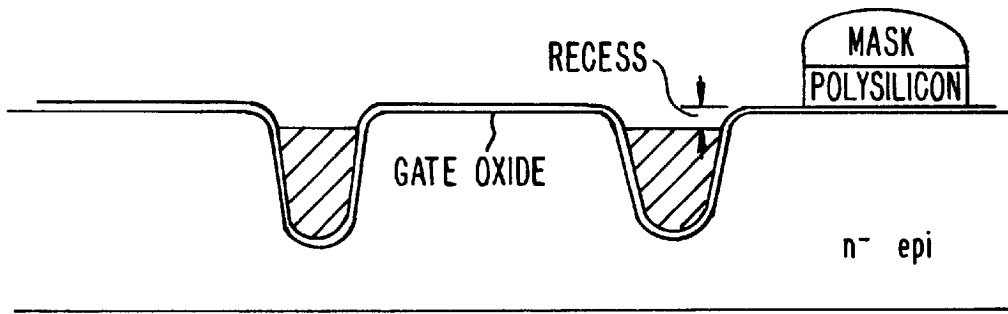
FIG. 4E.

**U.S. Patent**

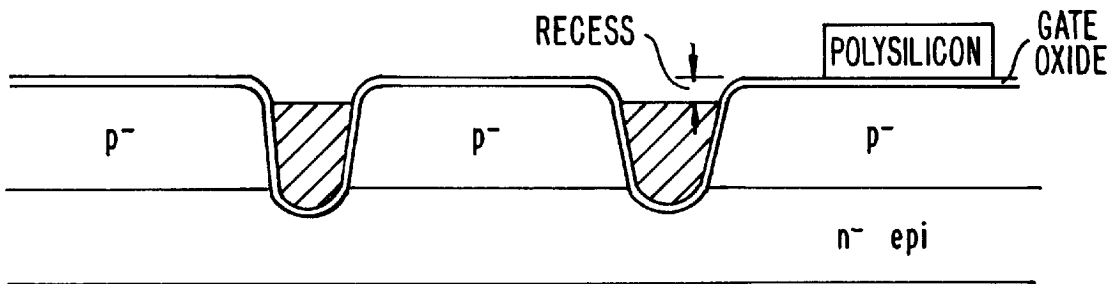
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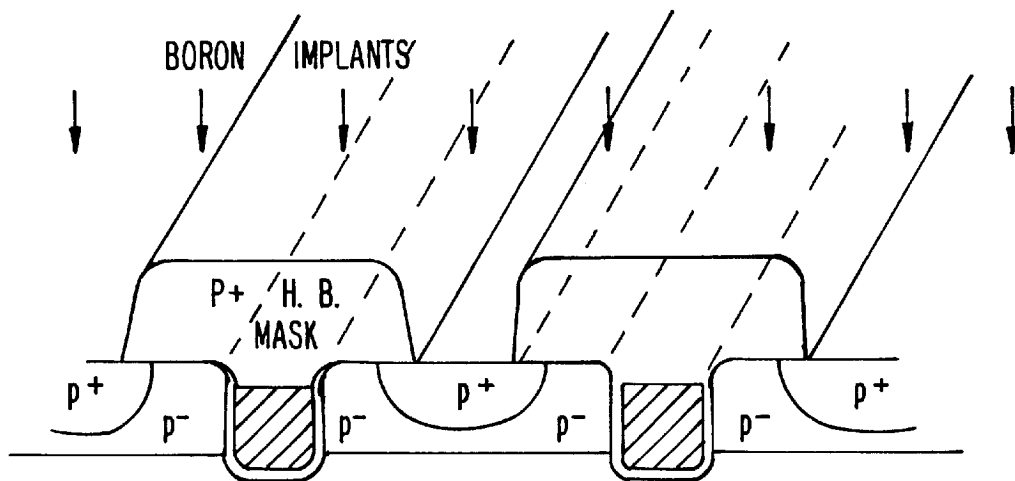
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**FIG. 4F.**



**FIG. 4G.**



**FIG. 4H.**

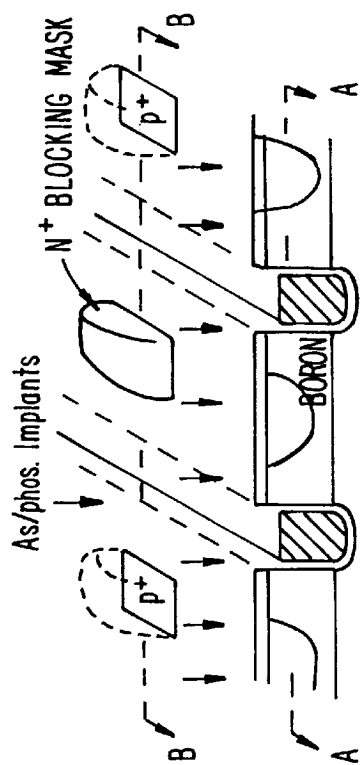


FIG. 4I.

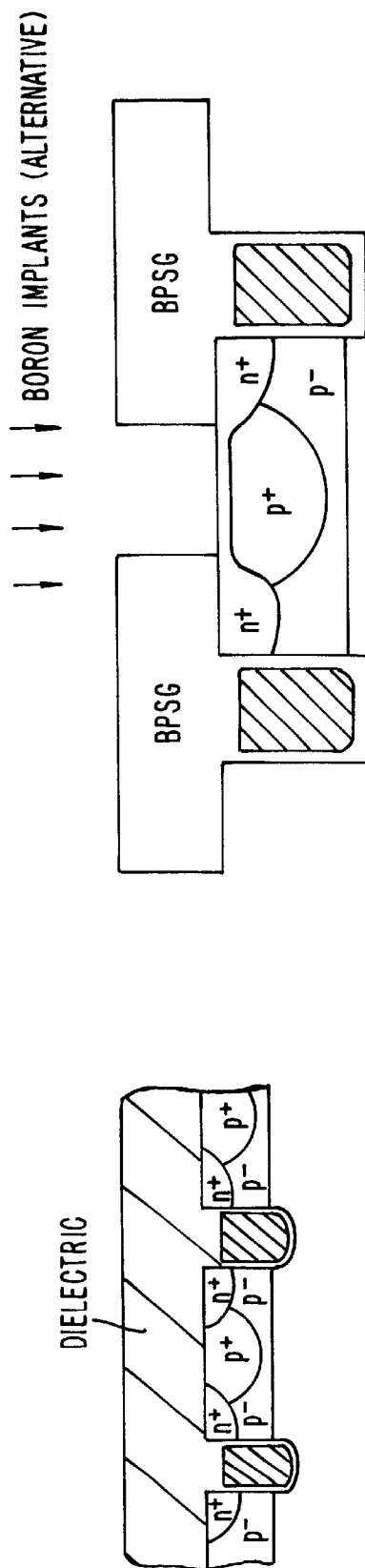
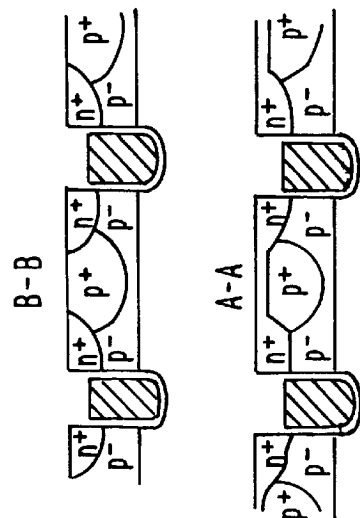


FIG. 4J.

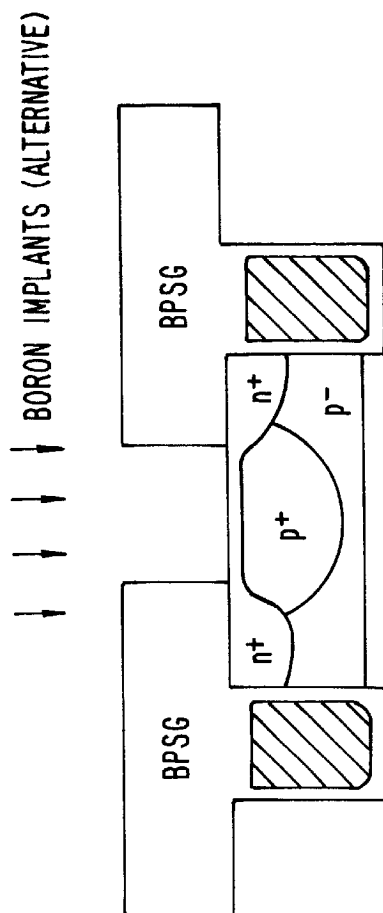


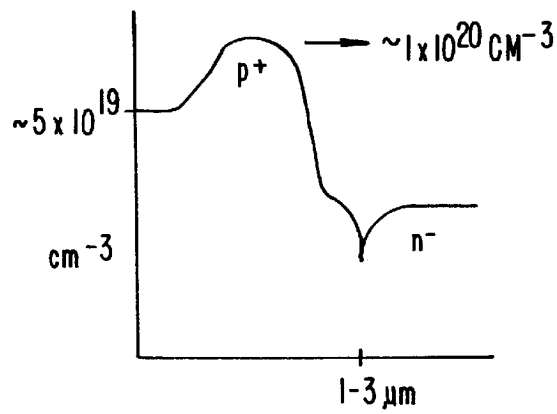
FIG. 4K.

**U.S. Patent**

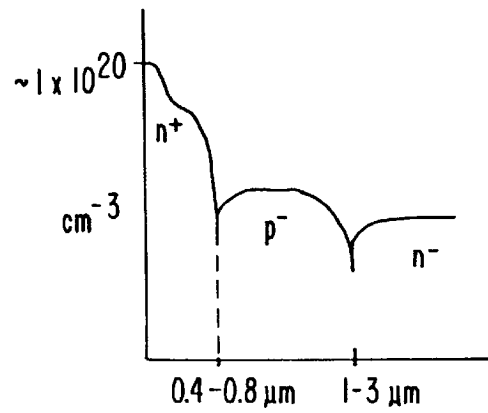
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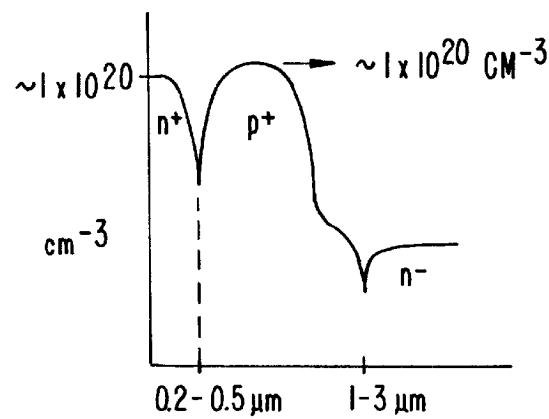
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**FIG. 5.**



**FIG. 5A.**



**FIG. 5B.**



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**FIELD EFFECT TRANSISTOR AND  
METHOD OF ITS MANUFACTURE**

This application is a continuation of and claims the benefit of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997 U.S. Pat. No. 6,429,481, the disclosure of which is incorporated herein by reference.

**BACKGROUND OF THE INVENTION**

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trench DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ( $R_{ds(on)}$ ) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which

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the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

**SUMMARY OF THE INVENTION**

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trench DMOS transistors exhibit low  $R_{ds(on)}$ , low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trench field effect transistor that includes

(a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped wells

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have a depth less than the predetermined depth of the trenches. The trenches have rounded top and bottom corners. There is an abrupt junction at the interface between each heavy body and the corresponding well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface. The array also includes a field termination structure surrounding the periphery of the array. The field termination structure includes a well having a depth greater than that of the gate-forming trenches. The field termination structure includes a termination trench extending continuously around the periphery of the array, more preferably a plurality of concentrically arranged termination trenches.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The field termination structure includes a doped well. The field termination structure includes a termination trench. The field termination structure includes a plurality of concentrically arranged termination trenches. Each of the DMOS transistor cells further comprises a doped heavy body and the doped heavy body extends into the semiconductor substrate to a depth that is less than the predetermined depth of the gate-forming trenches.

The invention also features a method of making a heavy body structure for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ . The second energy is from about 20 to 40 keV. The second dosage is from about  $1\text{E}14$  to  $1\text{E}15\text{ cm}^{-2}$ .

Additionally, the invention features a method of making a source for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about  $5\text{E}15$  to  $1\text{E}16\text{ cm}^{-2}$ . The second energy is from about 40 to 70 keV. The second dosage is from about  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ . The resulting depth of the source is from about 0.4 to  $0.8\text{ }\mu\text{m}$  the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trench field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning

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and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type to form a plurality of wells interposed between adjacent trenches, (g)

patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4–4k are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4–4k are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5, 5a and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trench DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1a, while the regions that have a p+ contact are shown in FIG. 1b.

As shown in FIGS. 1a and 1b, each trench DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n– epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to  $0.4\text{ }\mu\text{m}$ ). N+ doped source regions 32a, 32b are

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positioned one on each side of the trench **14**. A dielectric layer **35** covers the trench opening and the two source regions **32a**, **32b**. Extending between the source regions of adjacent cells is a p+ heavy body region **34** and, beneath it, a flat-bottomed p- well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1a** and **1b** includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p- well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in copending application U.S. Ser. No. 08/959,197, filed on Oct. 28, 1997. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p- well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and draws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3  $\mu\text{m}$  deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4-4k**. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4-4k**. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4-4k** can be varied. Moreover, some of the steps shown in FIGS. **4-4k** are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500  $\mu\text{m}$ , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10  $\mu\text{m}$ . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4-4c**. In FIG. **4**, an oxide layer is

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formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4a**, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of  $1\text{E}14$  ( $1 \times 10^{14}$ ) to  $1\text{E}16$   $\text{cm}^{-2}$ . As shown in FIG. **4b**, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4-4c**, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4d-4k**. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4d**). Preferably, as noted above, the trenches are formed using the process U.S. Application No. Ser. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4e**, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2  $\mu\text{m}$  depending on the trench width (shown by the dotted lines in FIG. **4e**). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 kÅ (indicated by solid lines in FIG. **4e**). The polysilicon is then doped to n-type, e.g., by conventional POCL<sub>3</sub> doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4f**. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4g**, the p- well is formed by implanting the dopant, e.g., a boron implant at an energy of



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30 to 100 keV and a dosage of  $1\text{E}13$  to  $1\text{E}15$ , and driving it in to a depth of from about 1 to 3  $\mu\text{m}$  using conventional drive in techniques.

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. 3. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4h. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4k, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ , and a second boron implant at an energy of 20 to 40 keV and a dose of  $1\text{E}14$  to  $1\text{E}15\text{ cm}^{-2}$ . The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1  $\mu\text{m}$  deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5  $\mu\text{m}$  deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1b), as shown in FIG. 4i. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4l, which correspond to FIGS. 1a and 1b).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of  $5\text{E}15$  to  $1\text{E}16\text{ cm}^{-2}$  followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of  $1\text{E}15$  to  $5\text{E}15\text{ cm}^{-2}$ . The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source

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regions will have a depth of about 0.4 to 0.8  $\mu\text{m}$  after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower  $R_{ds, on}$ .

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at  $900^\circ\text{C}$ ., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4j), after which the dielectric is patterned and etched (FIG. 4k) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A trench field effect transistor comprising:

- a semiconductor substrate having dopants of a first conductivity type;
- a trench extending to a first depth into said semiconductor substrate;
- a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;
- a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and
- a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;

wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

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2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.

5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.

6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.

7. The trenched field effect transistor of claim 1 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

8. The trenched field effect transistor of claim 7 wherein said deep doped region forms a PN junction diode with the substrate.

9. The trenched field effect transistor of claim 7 wherein the deep doped region forms a termination structure.

10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.

11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.

12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.

13. A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;

a pair of doped source junctions positioned on opposite sides of each trench, the source junctions having dopants of the first conductivity type;

a doped well having dopants of a second conductivity type with a charge opposite that of the first conductivity type, the doped well being formed in the semiconductor substrate between each pair of gate-forming trenches;

a heavy body formed inside the doped well and having a second depth that is less than the first depth of the trenches; and

heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

14. The field effect transistor of claim 13, wherein each said doped well has a substantially flat bottom.

15. The field effect transistor of claim 13 wherein the adjusted depth of the junction causes the breakdown origi-

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nation point to occur approximately halfway between adjacent gate-forming trenches.

16. The field effect transistor of claim 13 wherein each said doped well has a depth less than the first depth of said gate-forming trenches.

17. The field effect transistor of claim 13 wherein each said gate-forming trench has rounded top and bottom corners.

18. The field effect transistor of claim 13 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth greater than said first depth of the said plurality of gate-forming trenches.

19. The field effect transistor of claim 18 wherein the deep doped region forms a PN junction diode with the substrate.

20. The field effect transistor of claim 19 wherein the deep doped region forms a field termination structure surrounding the periphery of the plurality of gate-forming trenches.

21. The field effect transistor of claim 20 further comprising:

a layer of dielectric material formed over the deep doped region; and

a layer of conductive material formed on top of the layer of dielectric material.

22. The field effect transistor of claim 13 further comprising a field termination structure including a termination trench extending continuously around the periphery of the plurality of gate-forming trenches.

23. The field effect transistor of claim 22 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

24. The field effect transistor of claim 13 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.

25. The field effect transistor of claim 13 wherein said doped source regions extend along the length of the trench.

26. The field effect transistor of claim 25 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contacting the doped source regions.

27. The field effect transistor of claim 25 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.

28. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body is bounded by the pair of adjacent trenches and the doped source regions.

29. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.

30. The field effect transistor of claim 13 further comprising:

a layer of dielectric lining inside walls of each of said plurality of gate-forming trenches; and

a layer of conductive material substantially filling the gate-forming trenches.

31. The field effect transistor of claim 30 wherein the layer of conductive material comprises polysilicon.

32. The field effect transistor of claim 30 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.

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